Low-Power High-Speed SRAM Circuits using Low-Swing Bit-Lines

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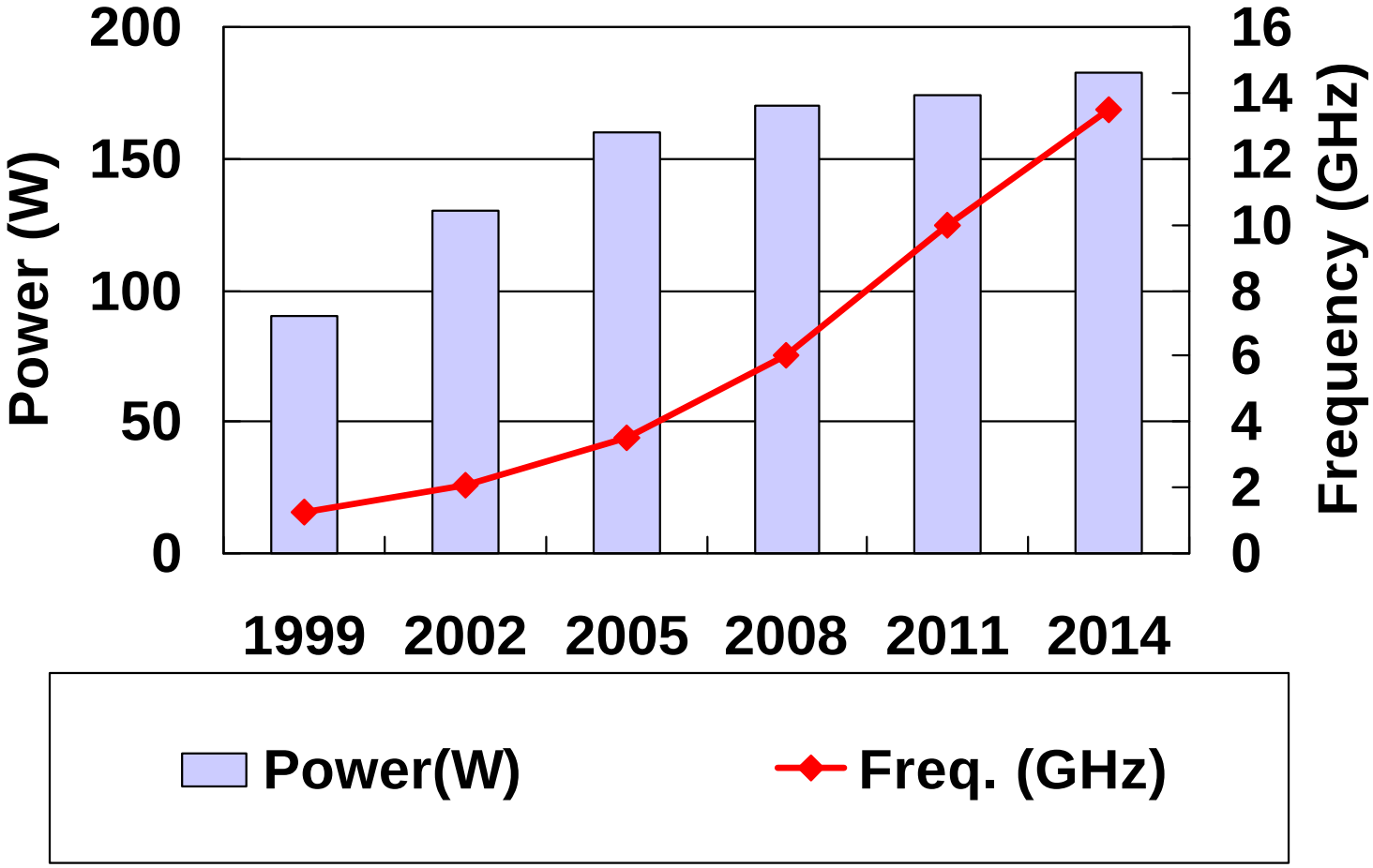
Contents

Power crisis in VLSI processor



(ITRS: International Technology Roadmap for Semiconductors 1999)

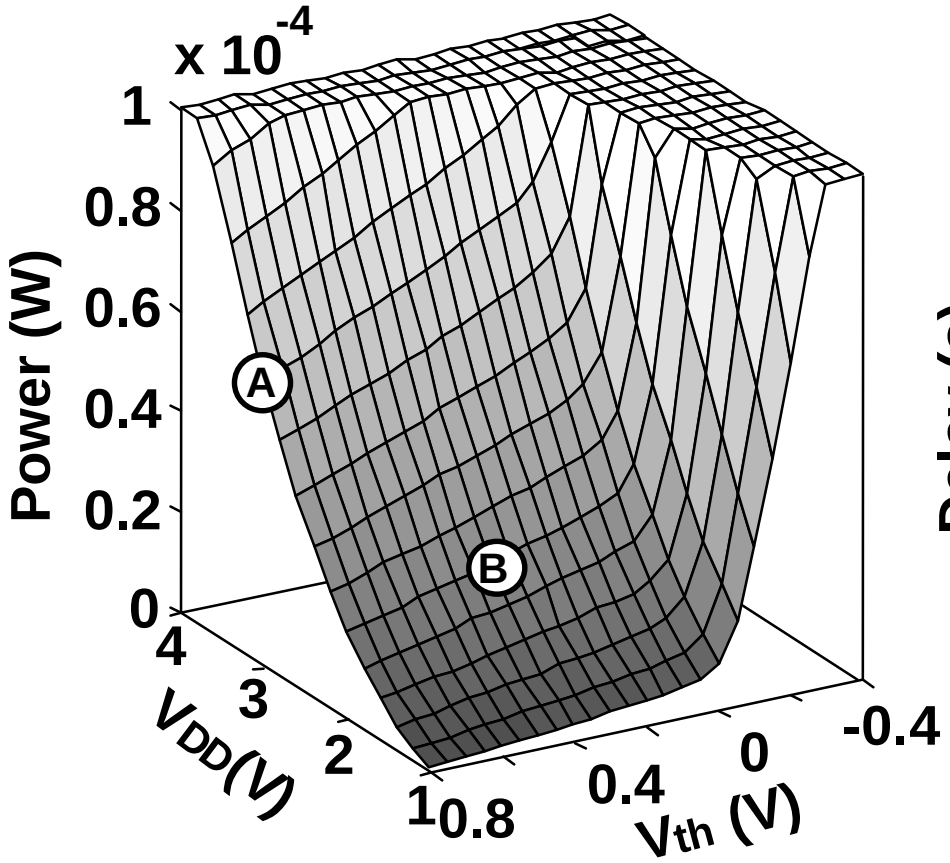
174W Power in 2011 acceptable?

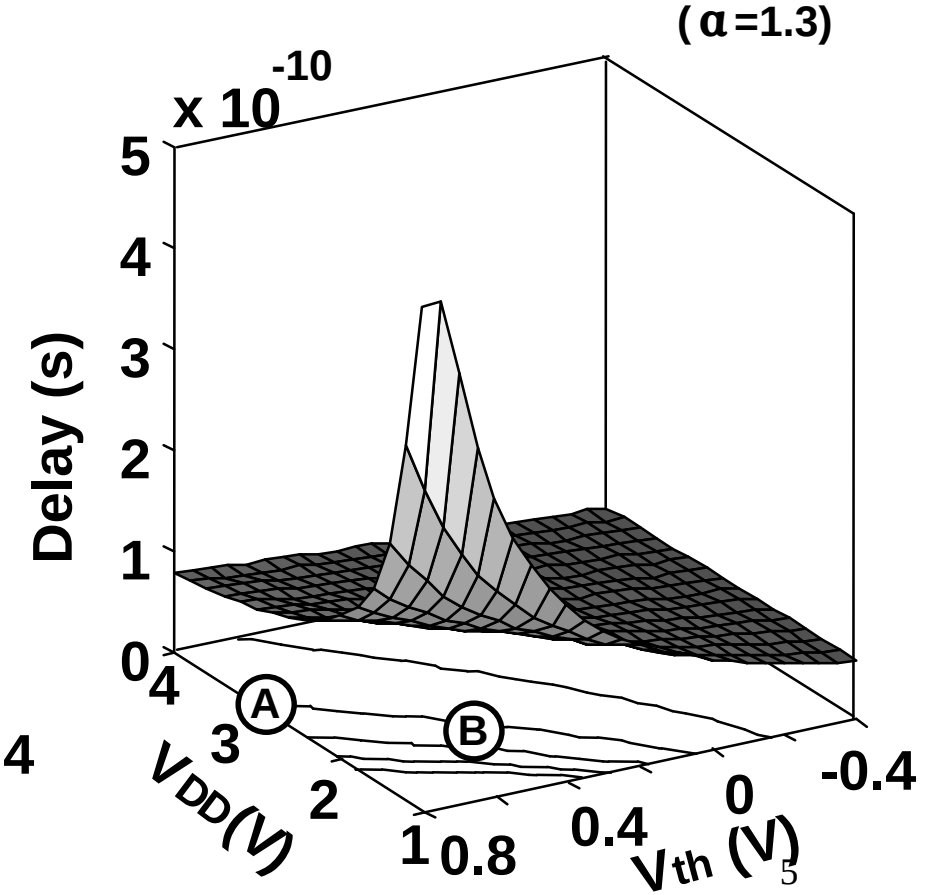
Contents

Power & delay dependence on V_{DD} & V_{TH}

$$P = P_t f_{CLK} C_L V_{DD}^2 + \text{Leak power}$$

$$t_{pd} = \frac{kC_L V_{DD}}{(V_{DD} - V_{TH})^{\alpha}} \quad (\alpha = 1.3)$$

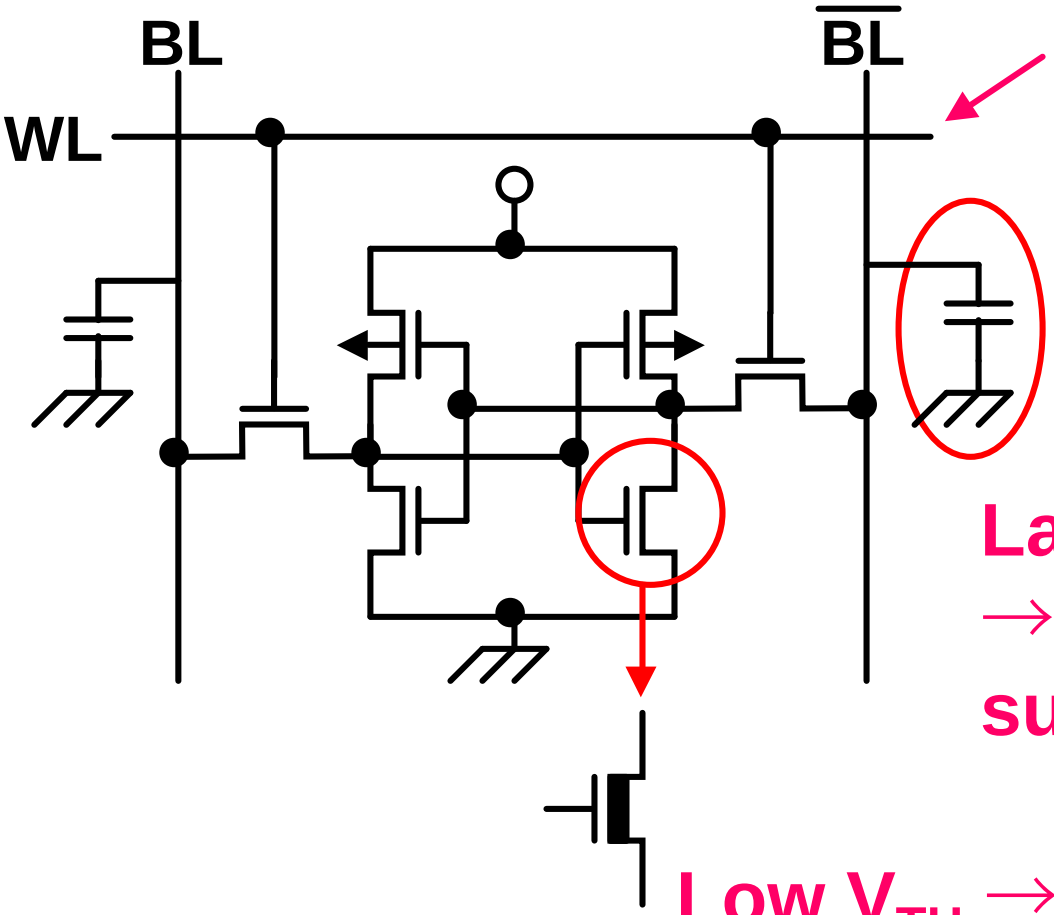




Contents

Low voltage SRAM memory cell

Lowering V_{DD} of SRAM cell is difficult.

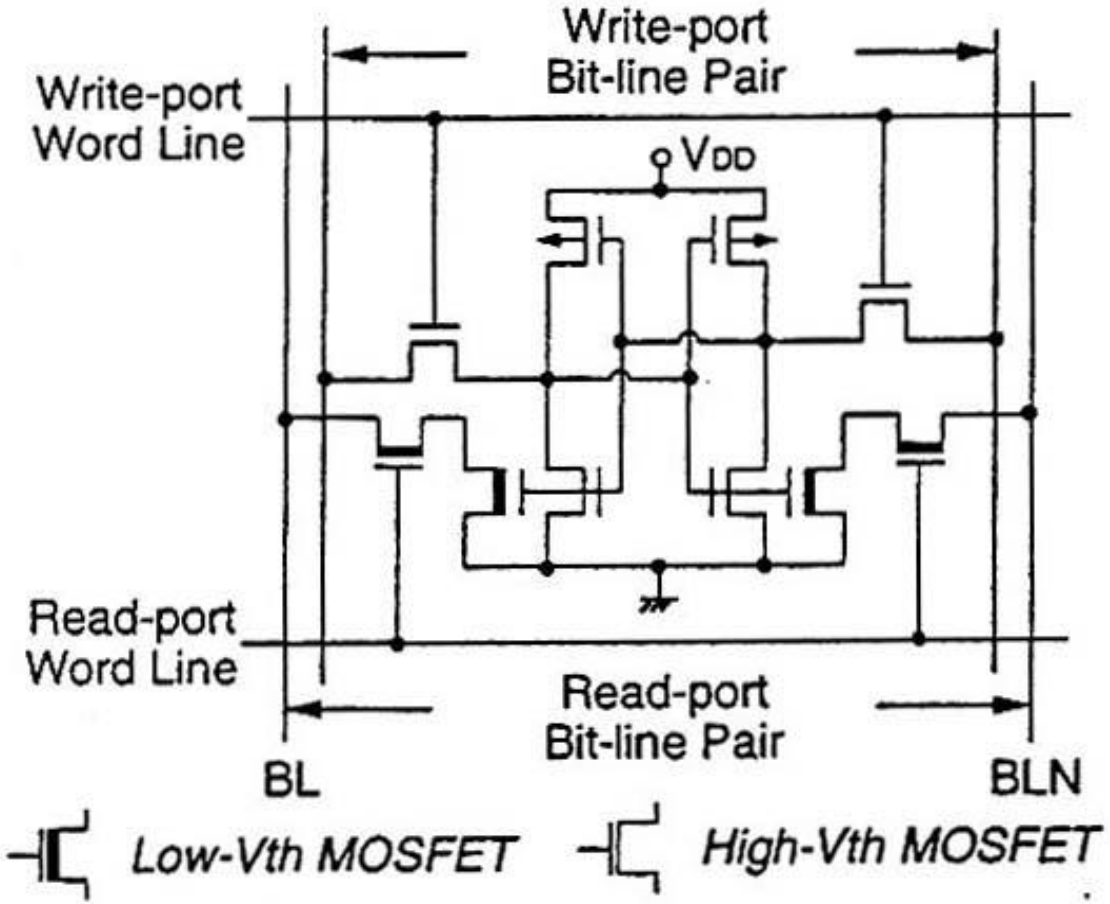


Long wire

Large capacitance → Needs strong current supply.

Low V_{TH} → Leak current

0.5-1V V_{DD} SRAM



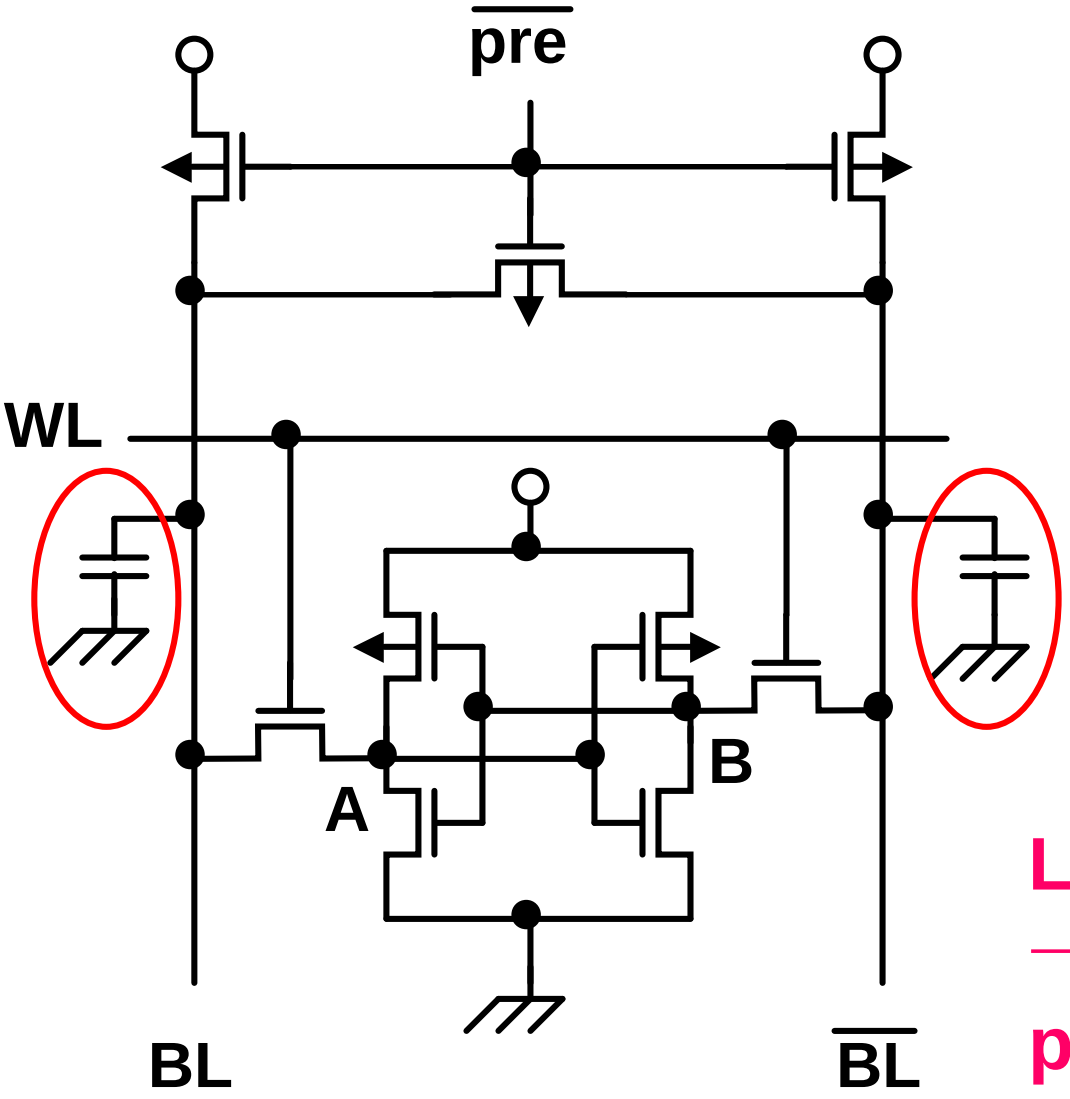
V_{DD}=0.5V
High-V_{TH}=0.35V
Low-V_{TH}=0.15V

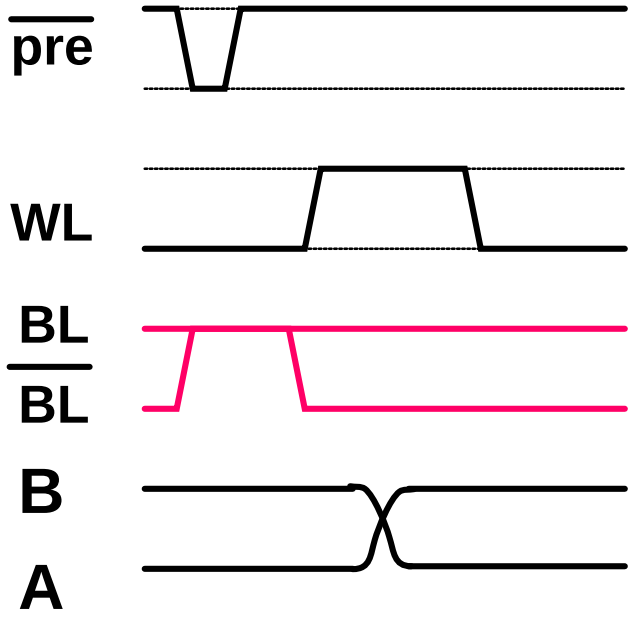
- Write-port and Read-port are divided in order to cut read error.
- Precharge level of Bit line is lower because of leakage at low-V_{TH} MOS.

Low precharge → Low speed
High-V_{TH}=0.35V → Leakage

(Takakuni Douseki et al., "A 0.5V-1V MTCMOS/SIMOX SRAM Macro with Multi-Vth Memory Cells", IEEE International SOI Conference, Oct., 2000)

Conventional SRAM

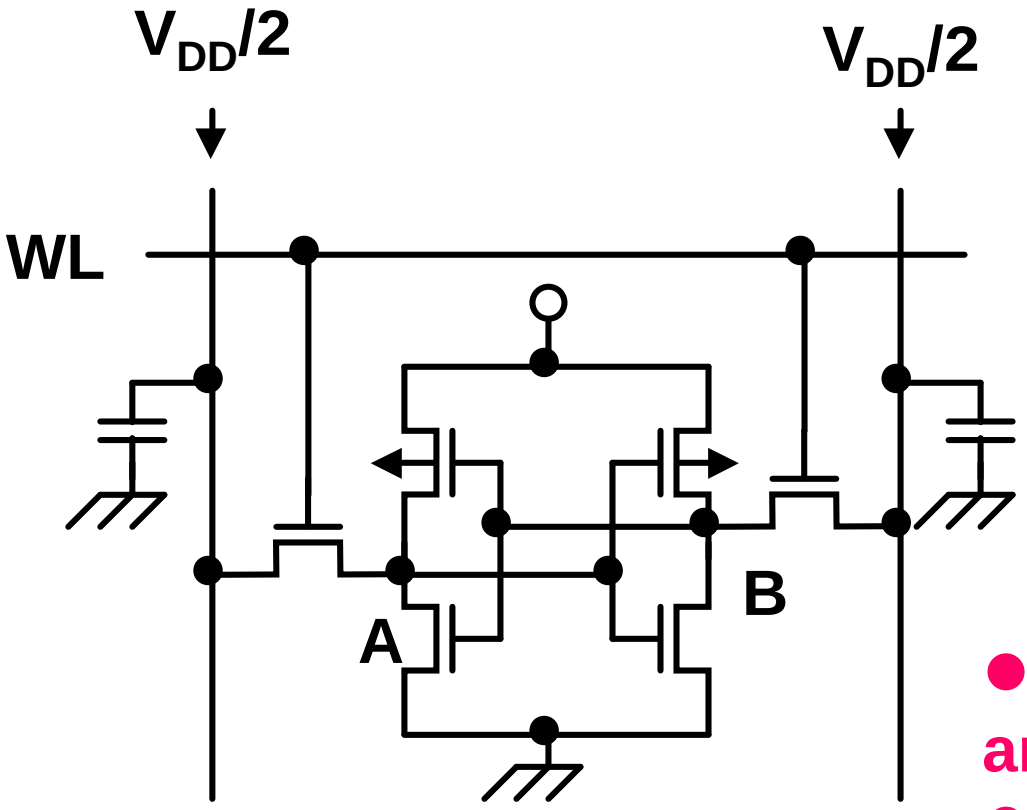


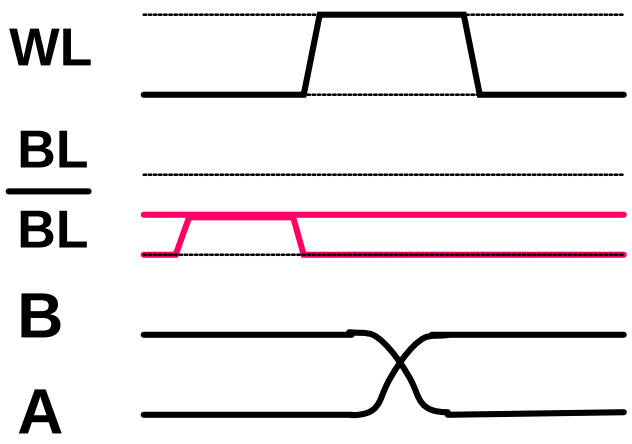


Write-cycle waveform

Large capacitance → Large power at precharge

SRAM cell using half-swing bit-lines



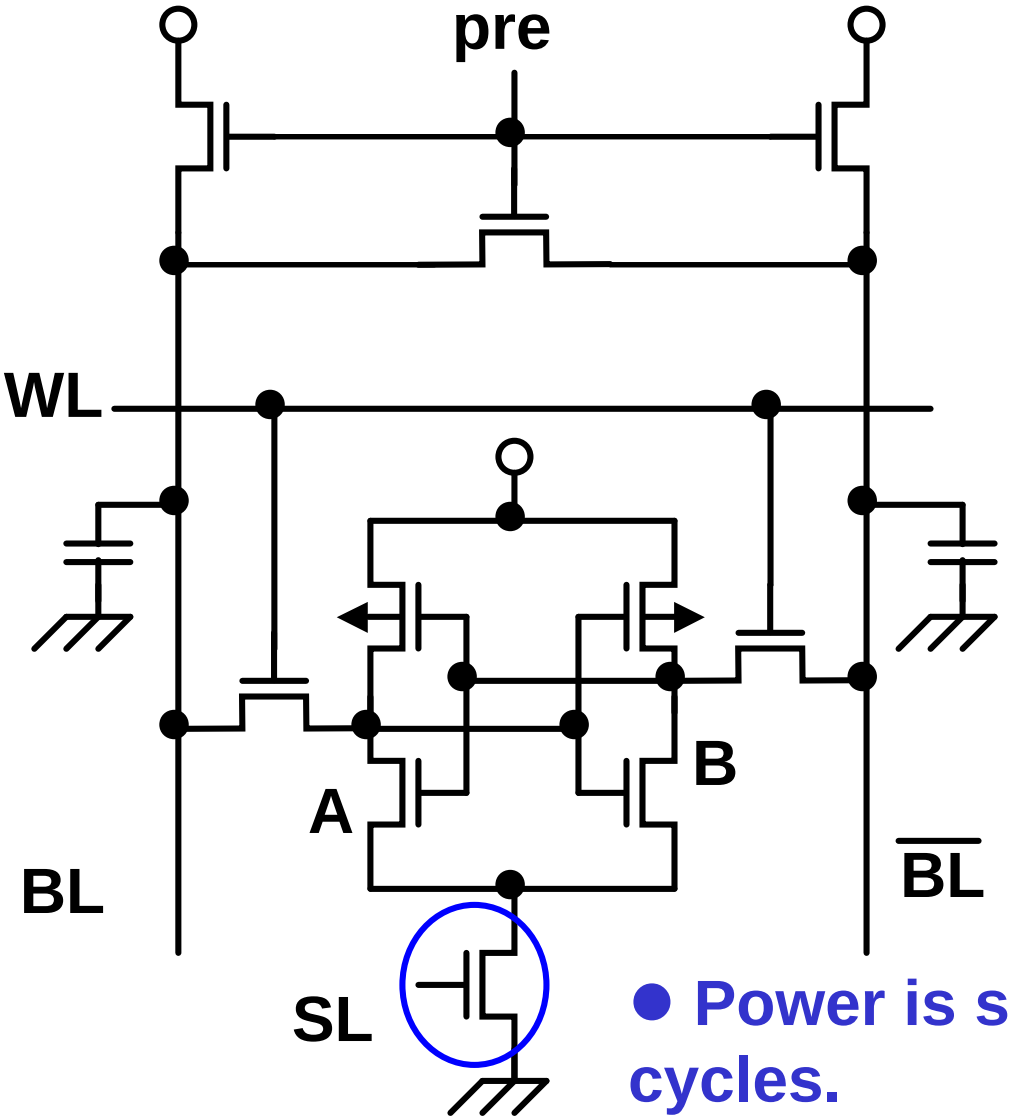


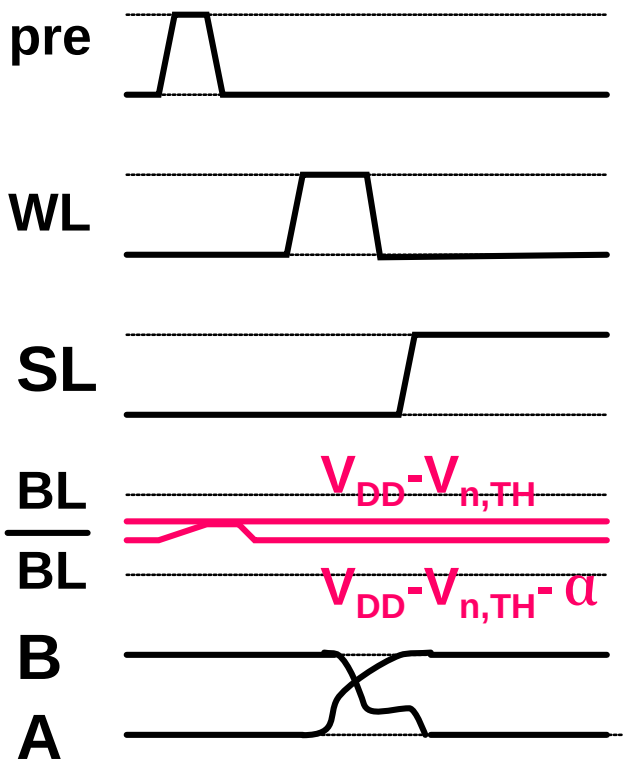
Write-cycle waveform

- Power isn't saved in write and read cycles.
- Swing level cannot be lowered below $V_{DD}/2$.

(Mark A. Horowitz et al.,
"Low-power SRAM Design Using Half-Swing Pulse-mode Techniques",
IEEE Journal of SSC, Vol.33, No.11, Nov., 1998)

SRAM cell using low-swing bit-lines

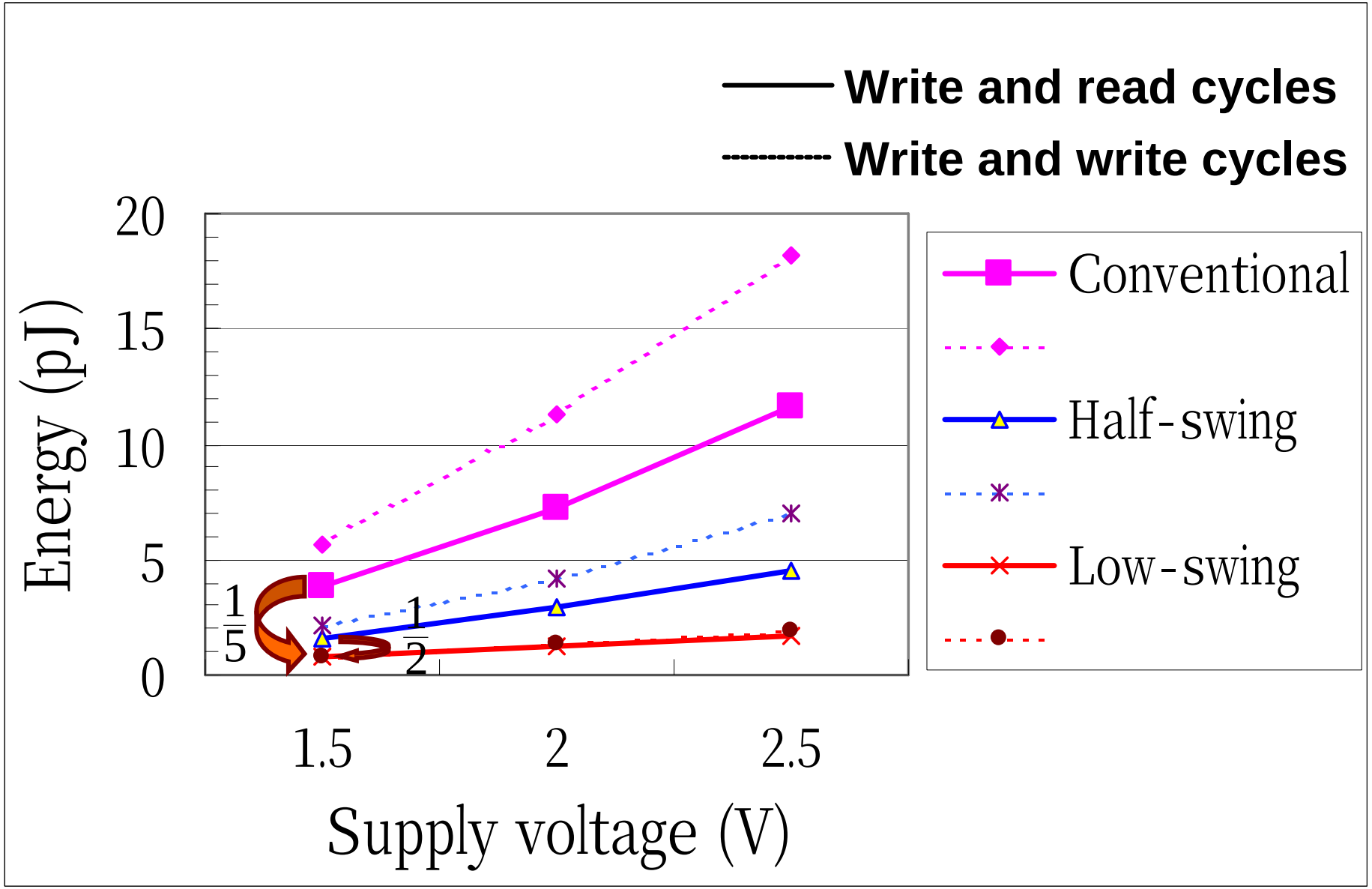




Write-cycle waveform

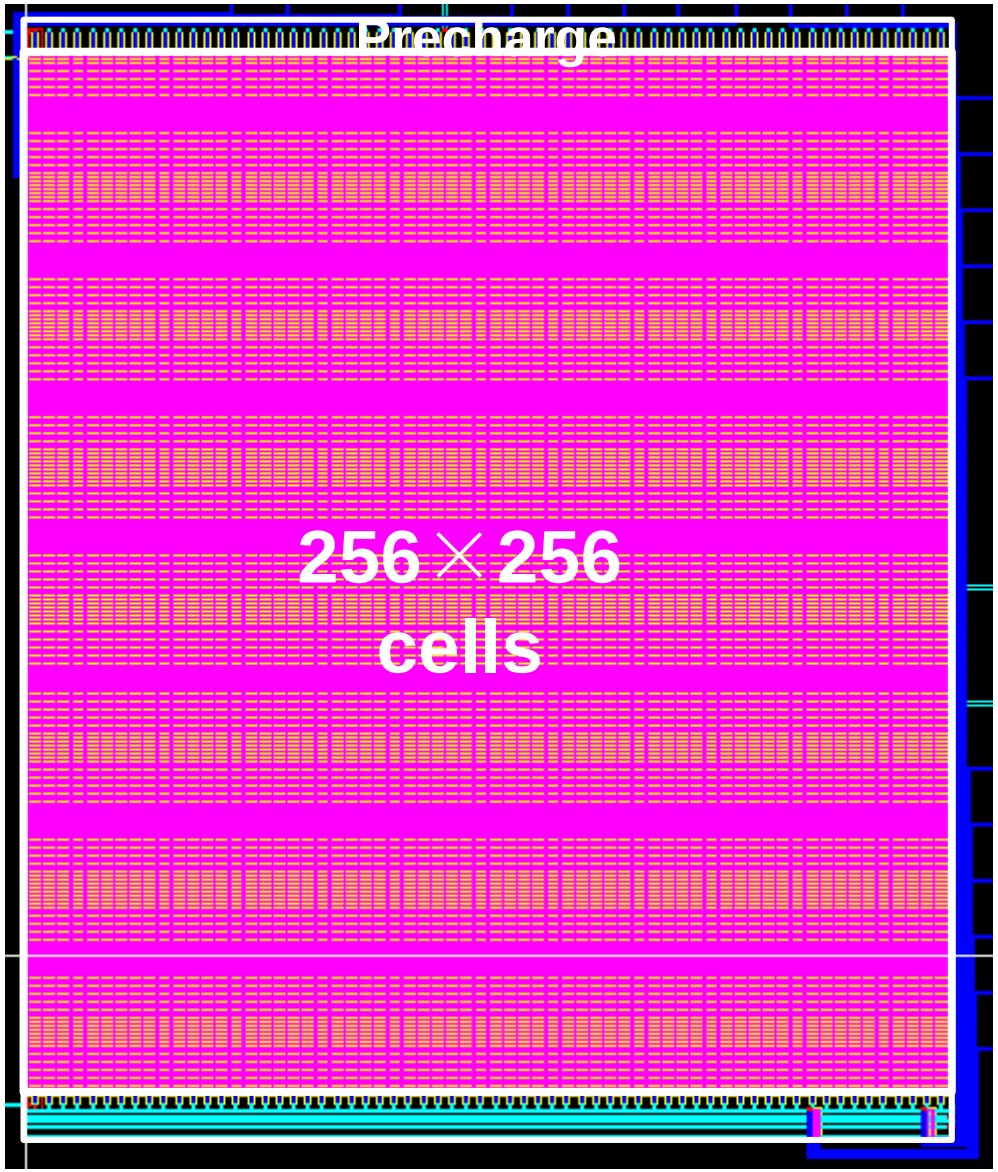
- Power is saved in write and read cycles.
- Can be lowered below $V_{DD}/2$.

Simulation result of energy consumption

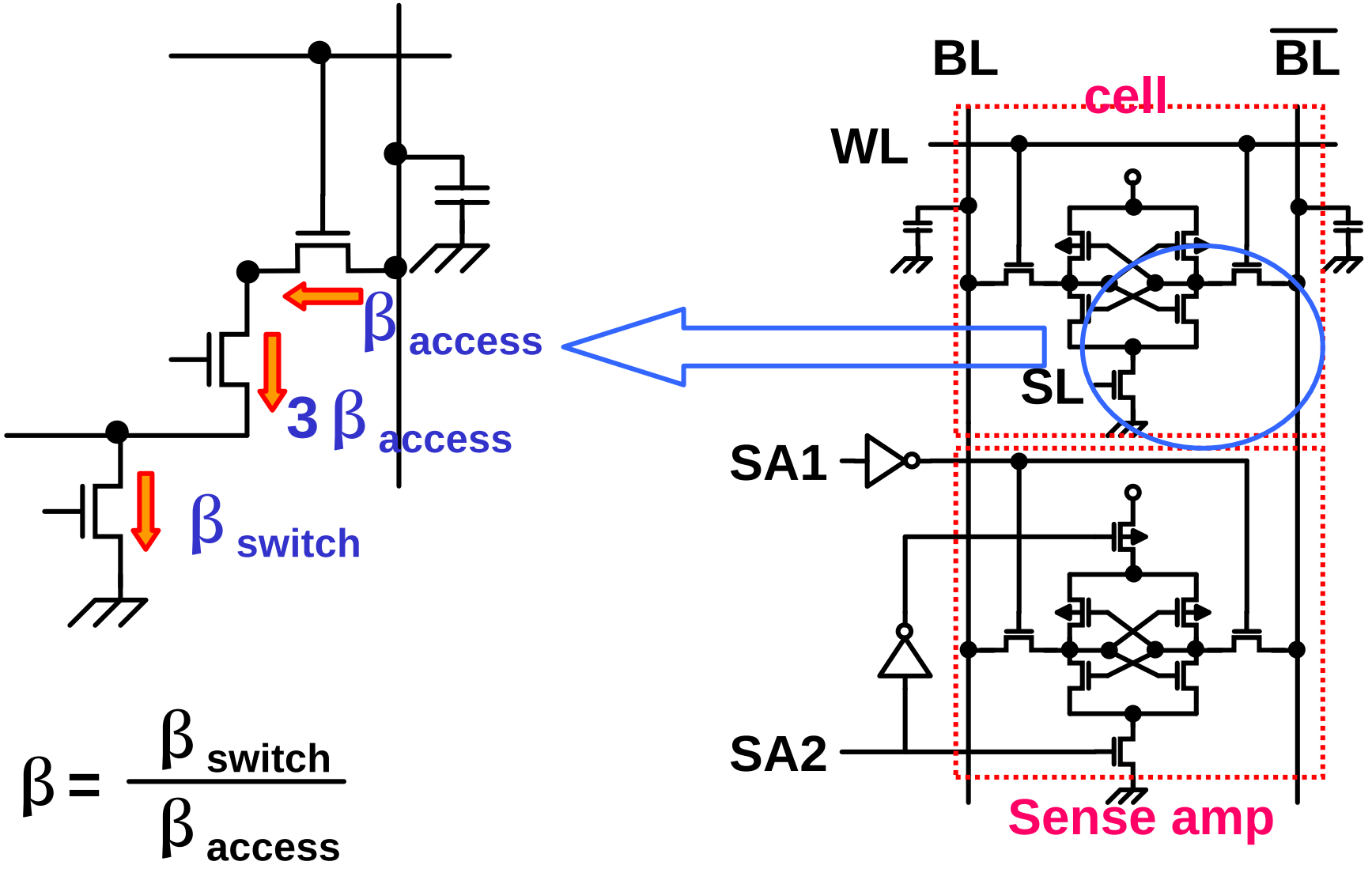


Layout pattern of SRAM cells

Technology	0.35μm CMOS 3-metal (Rohm)
Organization	256×256 cells
Supply voltage	1.5V～2.5V
Core size	4.0mm²
Cell size	55.3μm²

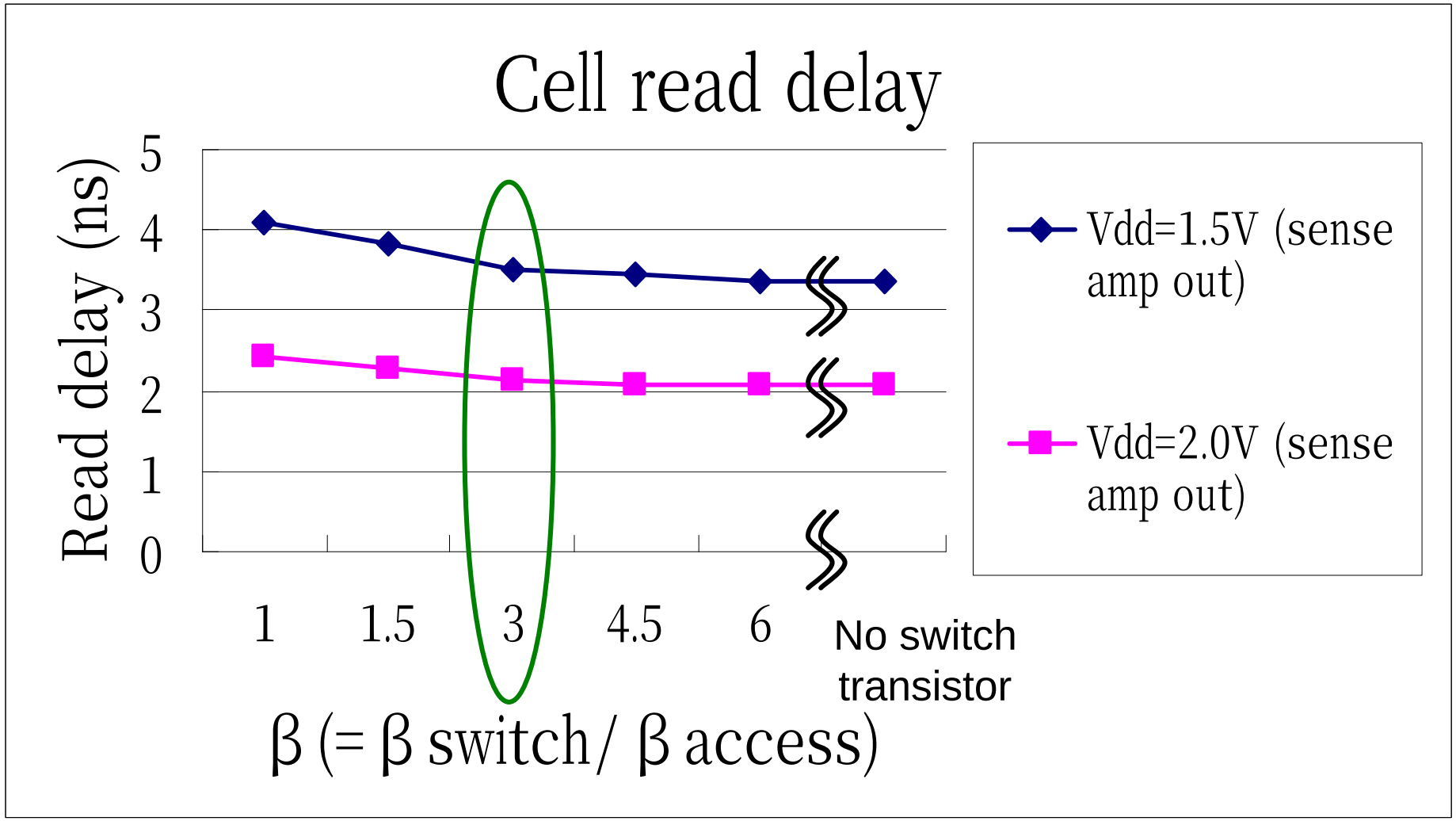


Evaluation of read delay

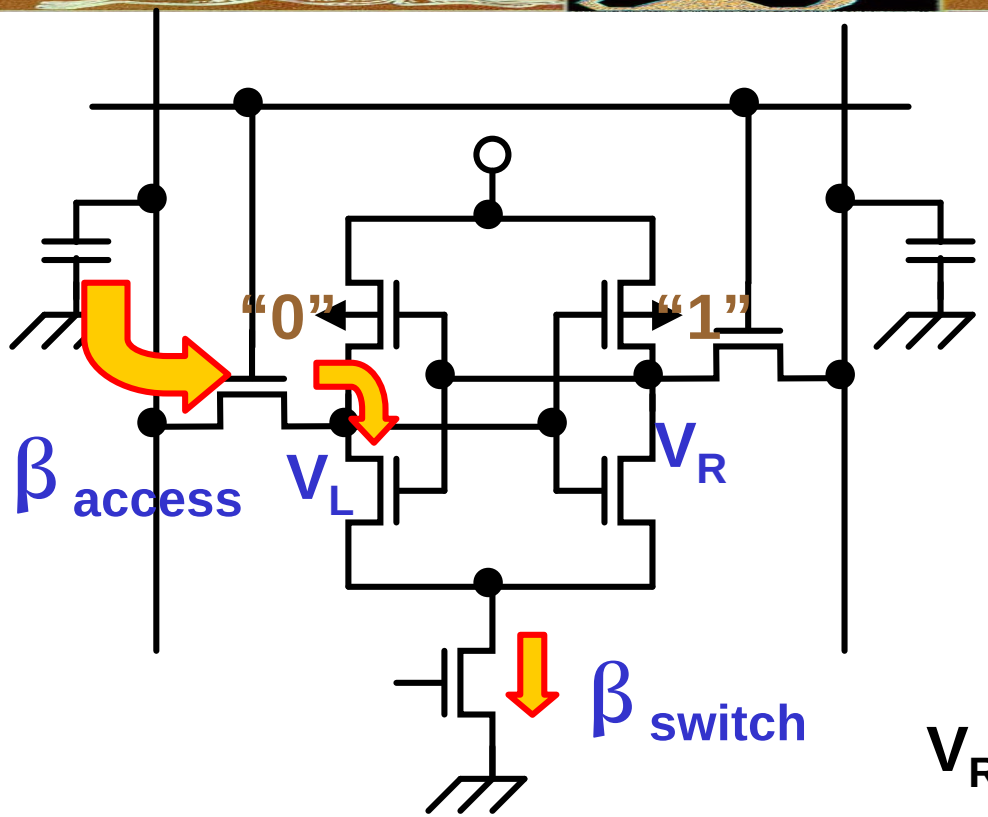


$$\beta = \frac{\beta_{switch}}{\beta_{access}}$$

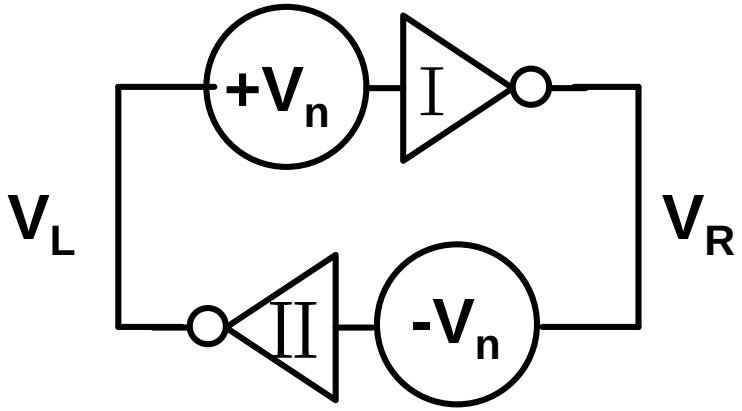
Simulation result of cell read delay

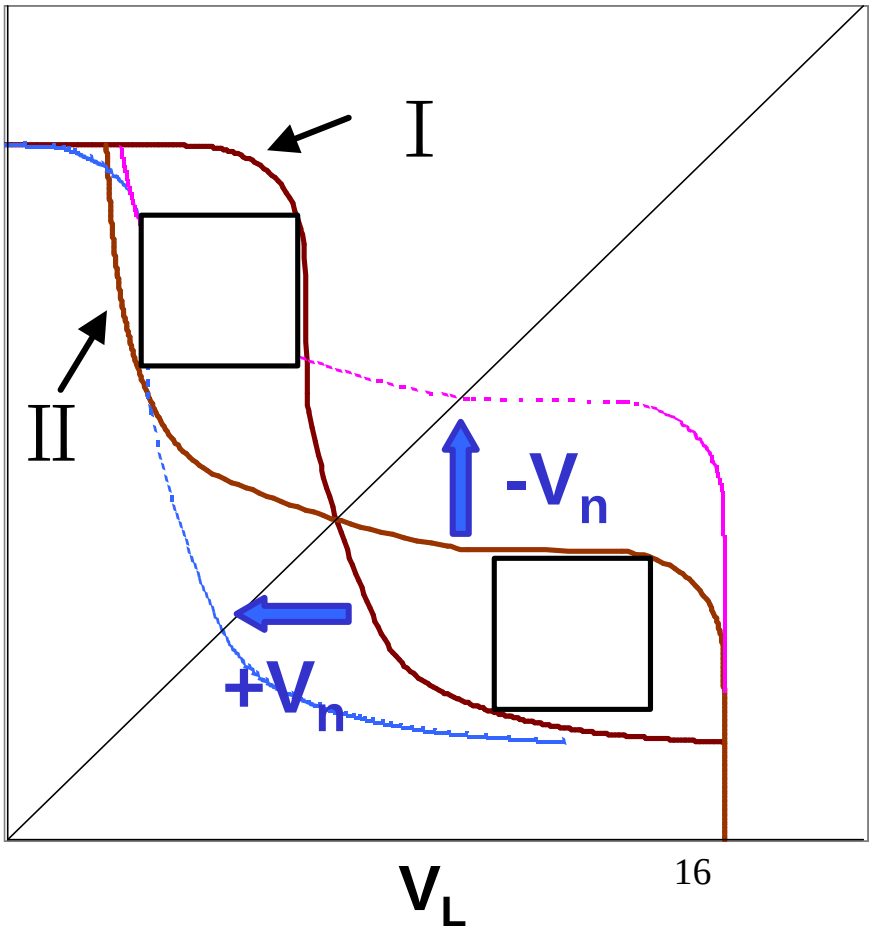


Analysis of static noise margin

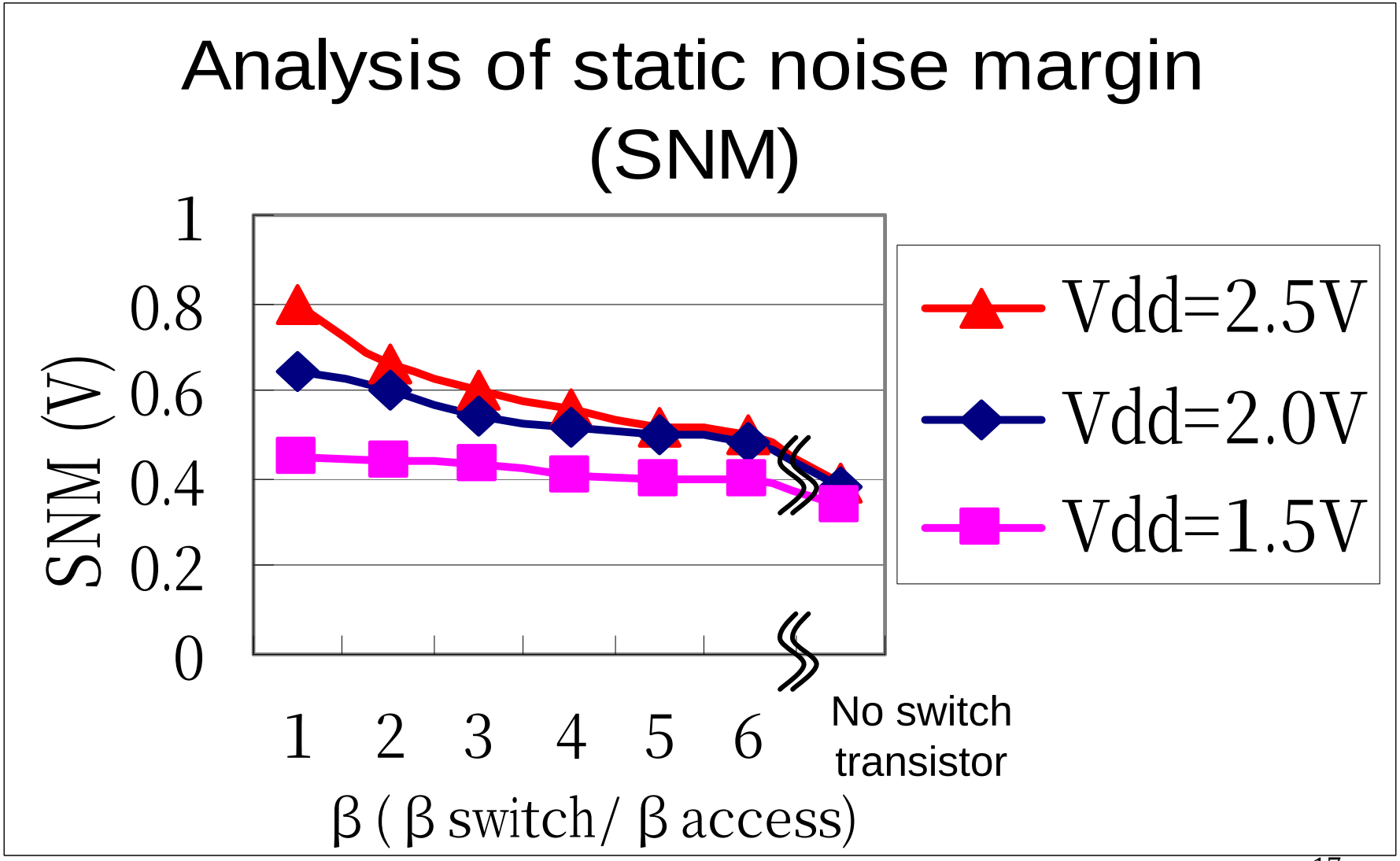


$$\beta = \frac{\beta_{switch}}{\beta_{access}}$$

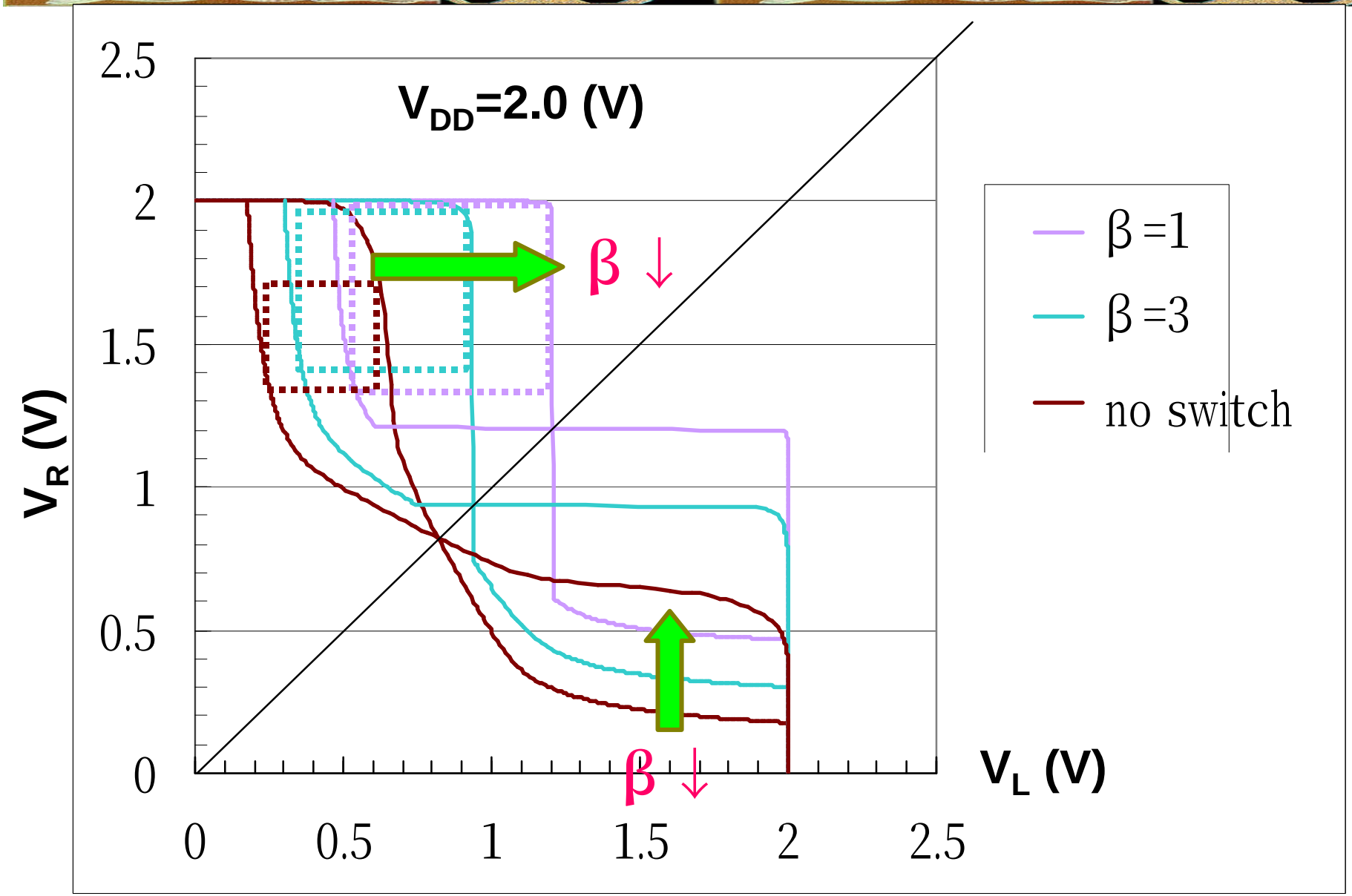




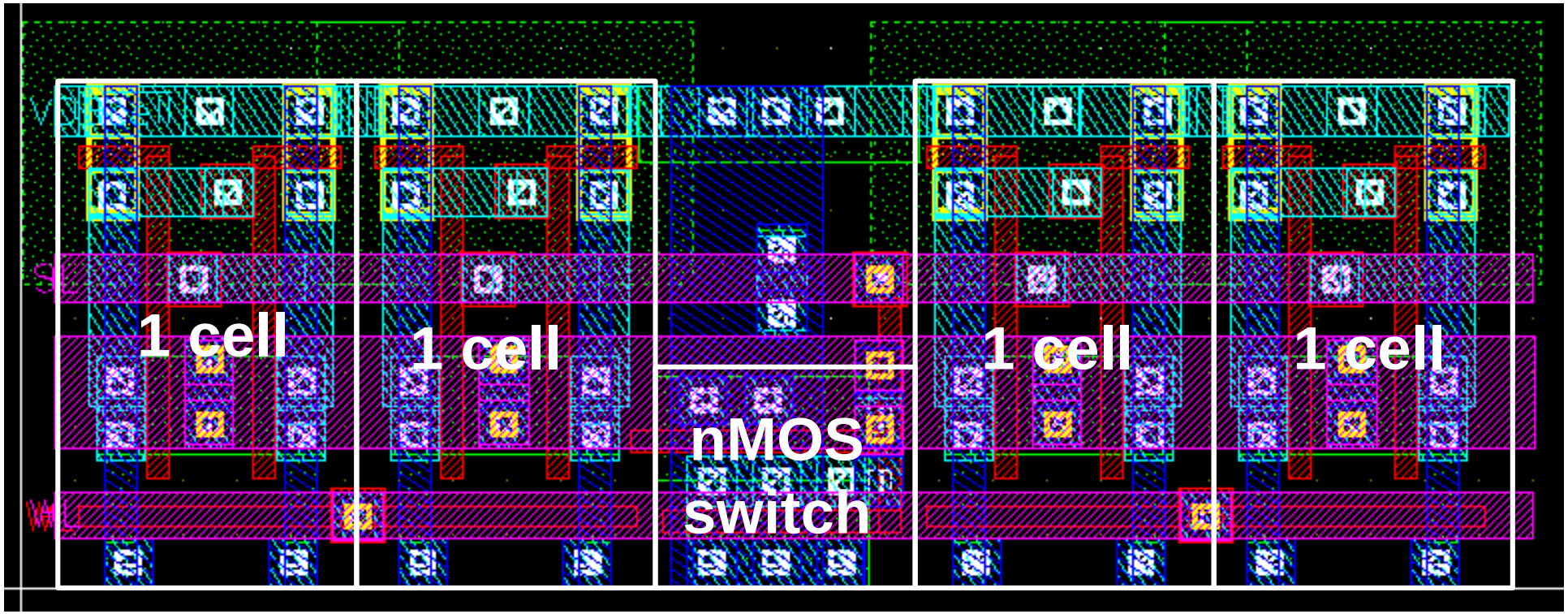
Simulation result of static noise margin



Input-output characteristic of inverters

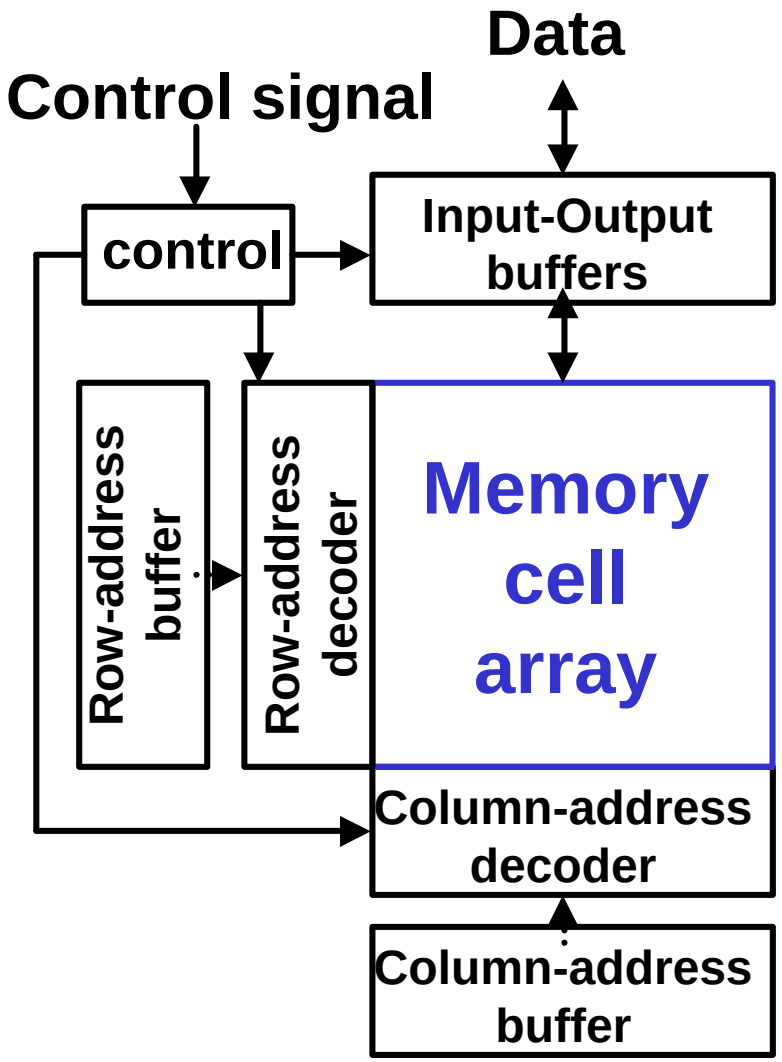


Layout pattern of 4 cells



11% large area

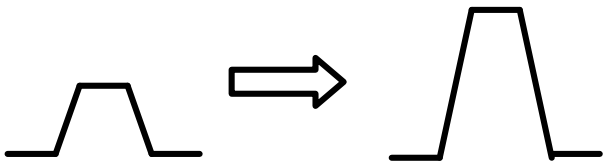
An SRAM architecture



Logic
V_{DD}=0.5V

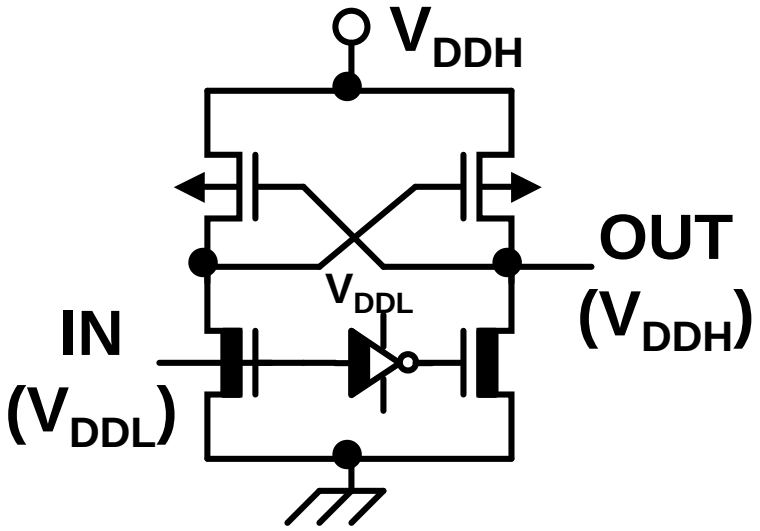
High speed level converter is needed.

Memory
V_{DD}=1.0V～1.5V

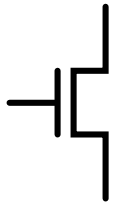


Level converters (0.5V → 1.0V)

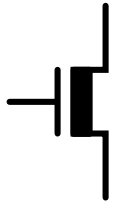
Conventional



V_{DDH} : High V_{DD}
V_{DDL} : Low V_{DD}



High-V_{TH} MOS

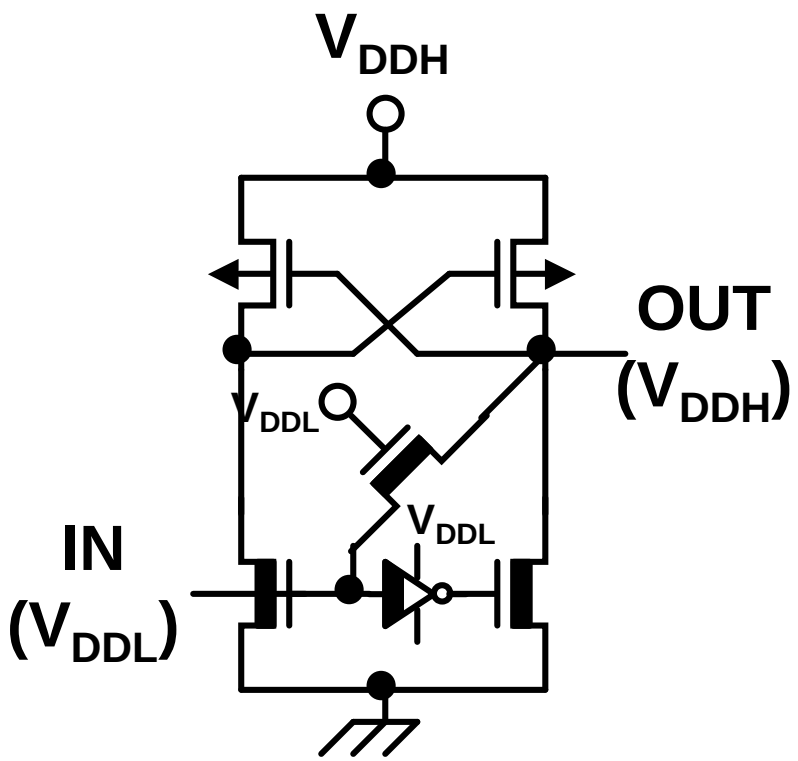


Low-V_{TH} MOS

Rising delay : 1ns
Falling delay : 1ns

Level converters (0.5V → 1.0V)

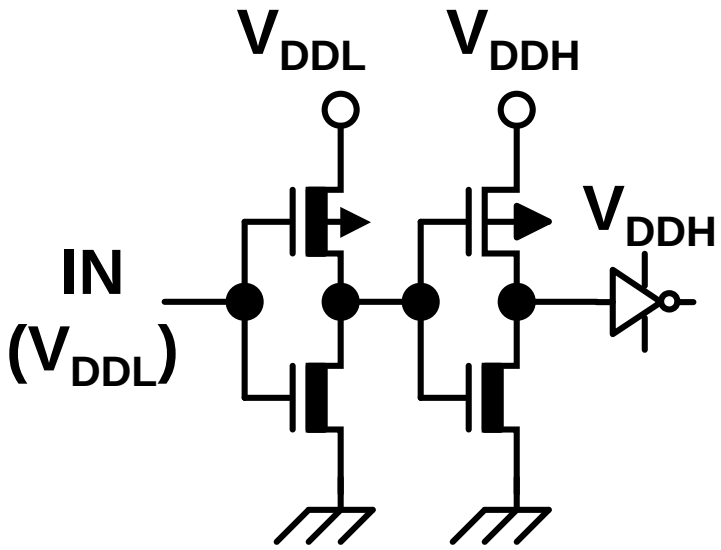
Proposed



Falling delay : 0.4ns

Power increase

Proposed (Inverter type)



Rising delay : 0.6ns

Power increase

Summary

Power crisis in VLSI processor

→ Low-power logic technologies

→ Low-power SRAM technologies

Low-swing bit line
80% power saving at V_{DD}=1.5V
11% area increase
5% delay increase at V_{DD}=1.5V

Logic : Low-V_{DD}
Memory : High-V_{DD}
→Needs high-speed level converter.

Future works

Improvement of design

- **Area**
  → **Improvement of layout**
- **Delay**
  → **High-speed level converter**

Logic design

Decoder, buffer, control

Measurement

- **Characteristic**
- **Power**
- **Delay**

Low-power High-speed SRAM circuit as a memory for 0.5V 1GHz processor