0.5V VLSI Processor Circuit Technologies

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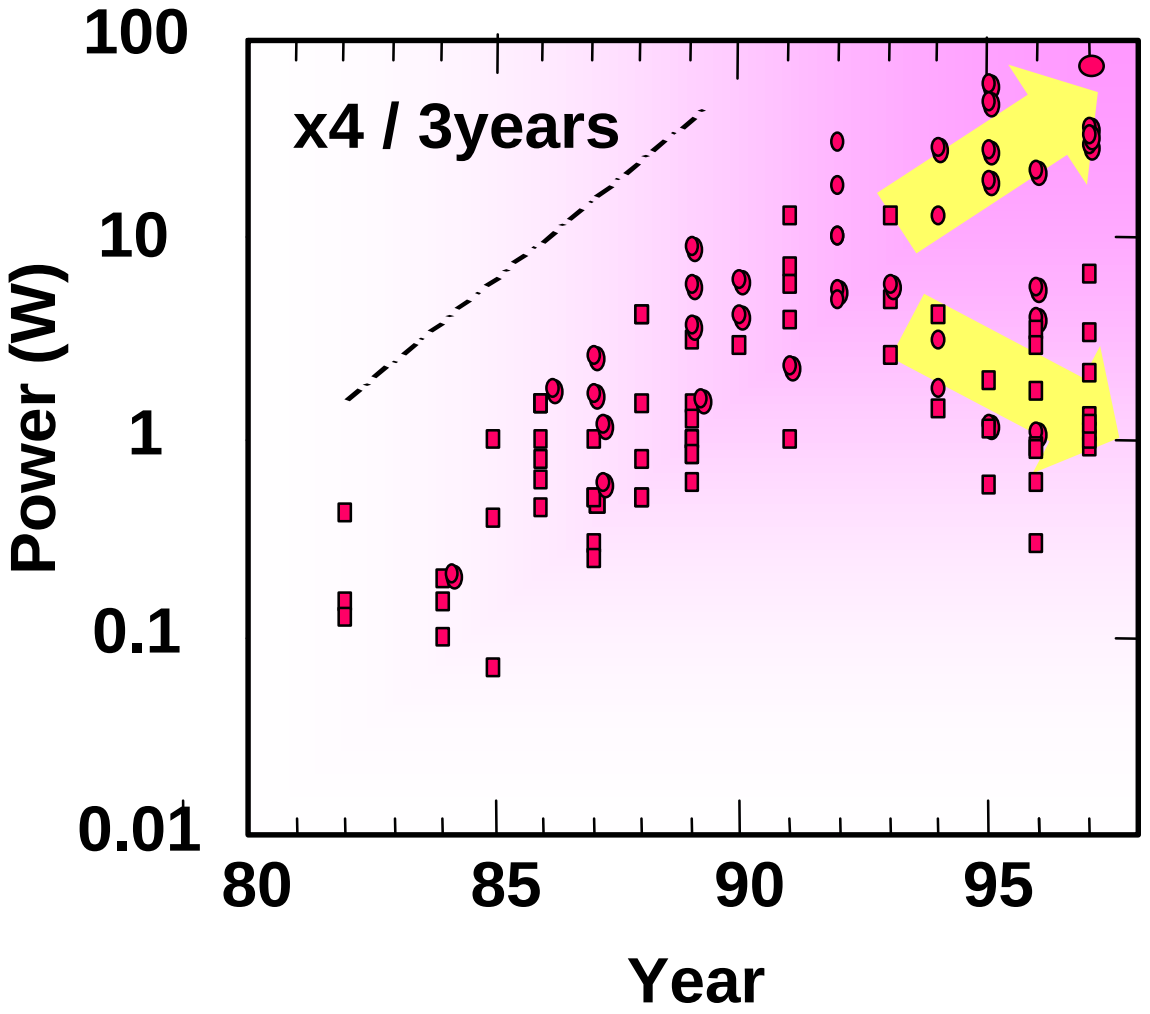
Contents

Trend of processor power

(Power consumption of processors published in ISSCC)

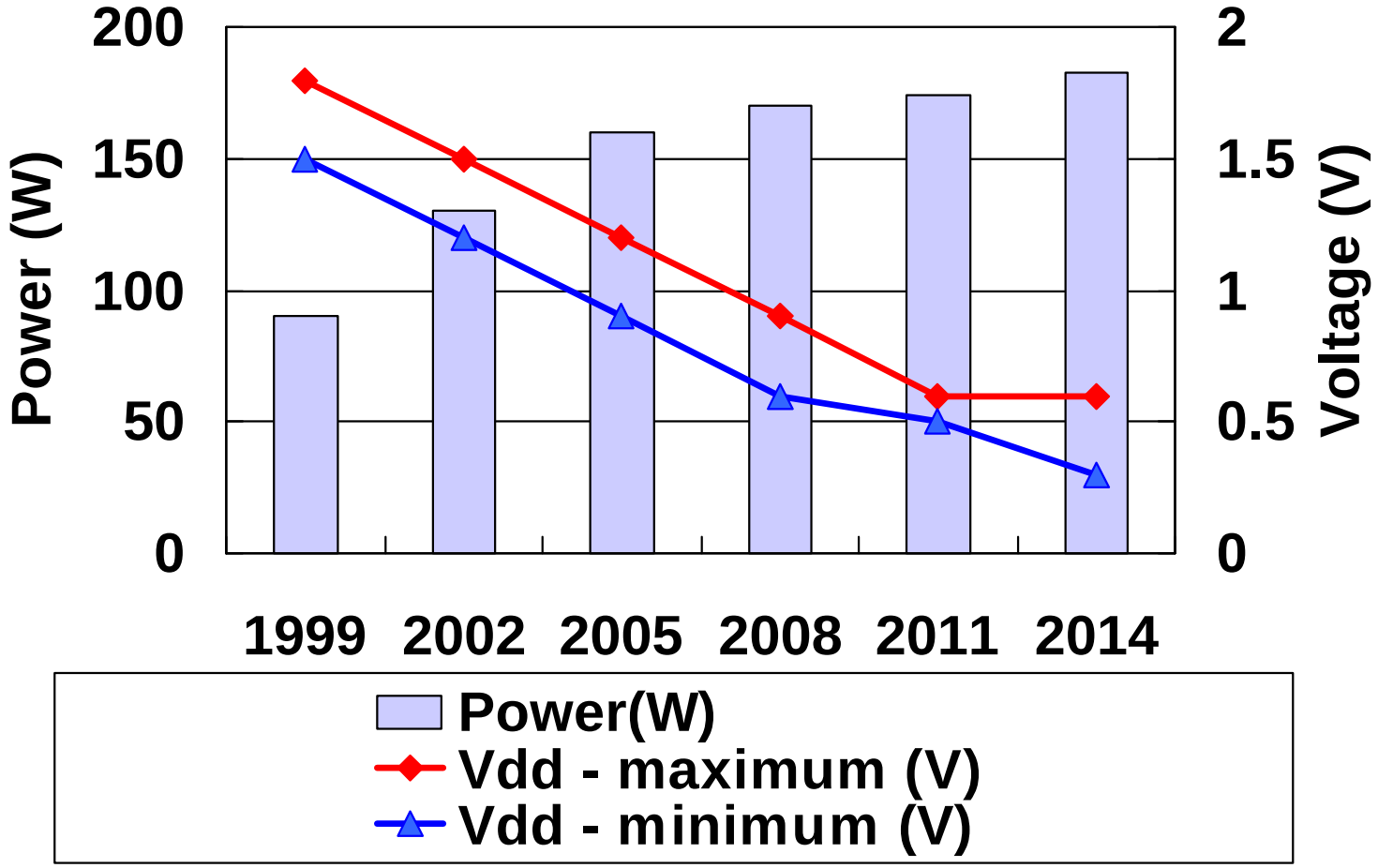


Very High speed
Large power

High speed
Low power

Crusoe
Published in Jan, 2000
Power < 6W

Power Crisis in VLSI processor



(ITRS: International Technology Roadmap for Semiconductors 1999)

174W Power in 2011 acceptable?

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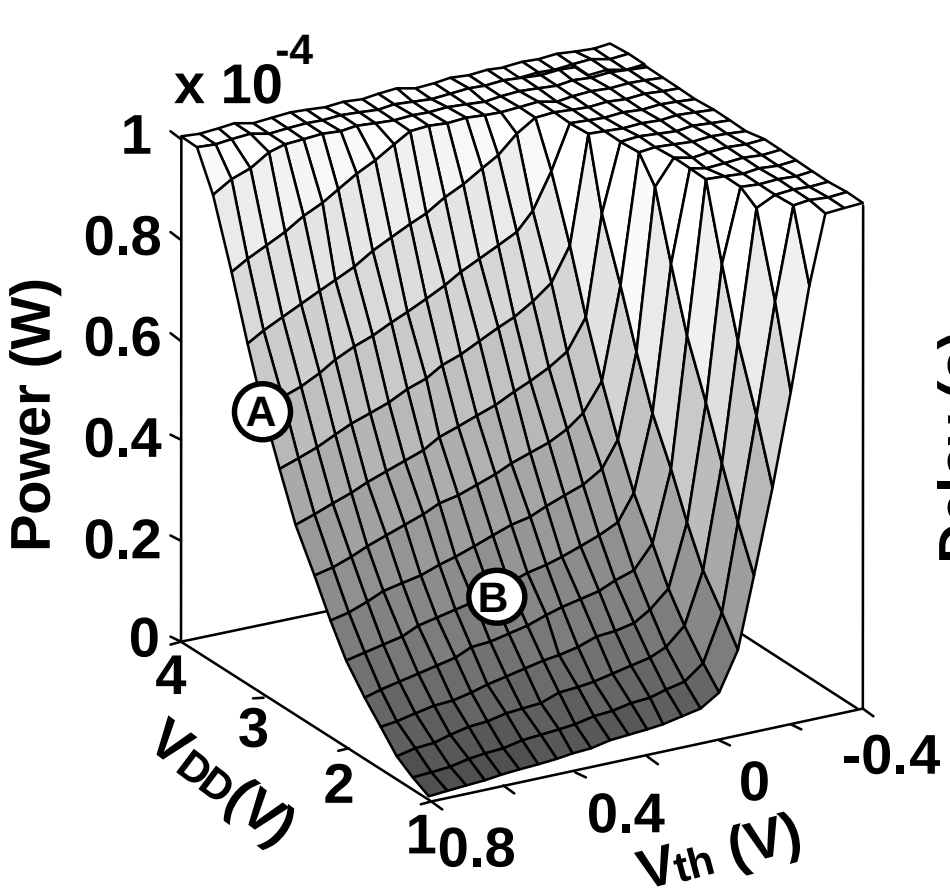
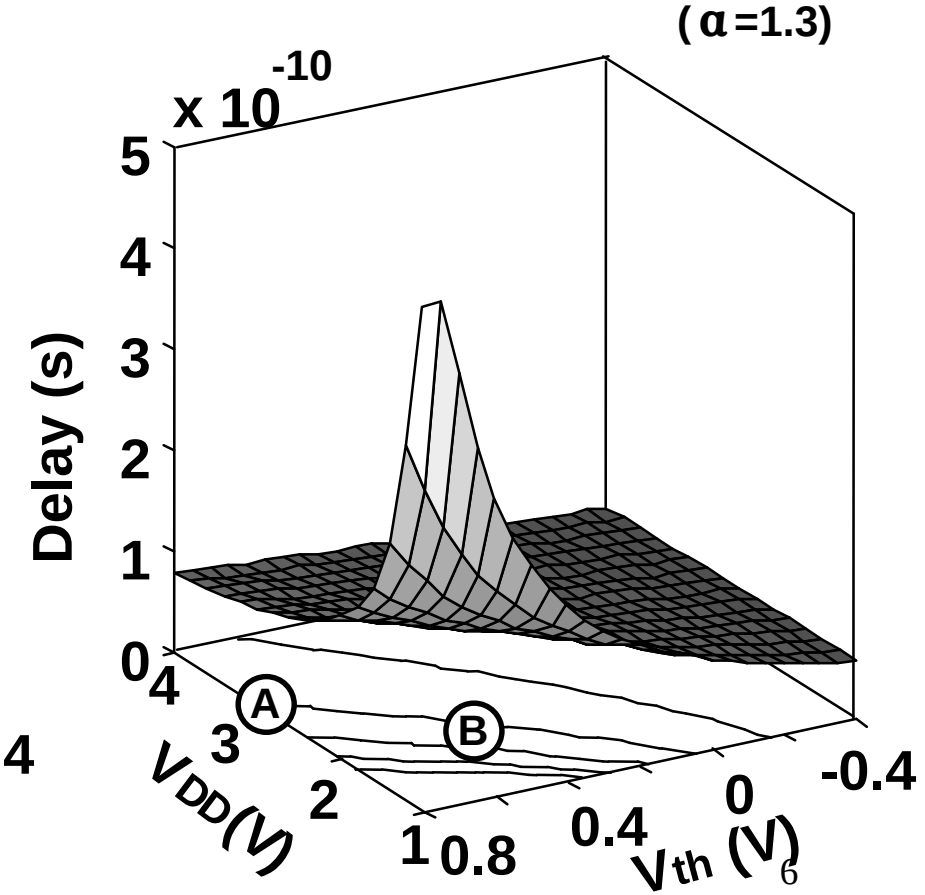
Power & Delay Dependence on V_{DD} & V_{TH}

$$P = P_t f_{CLK} C_L V_{DD}^2 + \text{Leak power}$$

$$t_{pd} = \frac{kC_L V_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$





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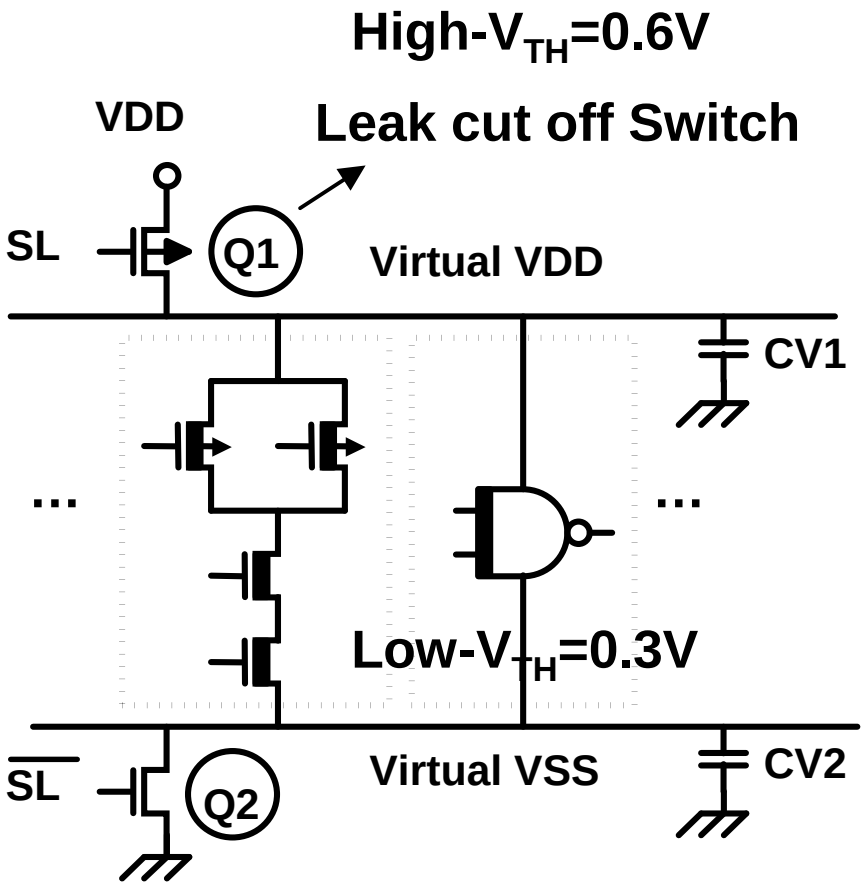
Controlling V_{DD} and V_{TH} for low power

	Active Power	Standby Power
Multiple V_{TH}	Dual-V_{TH}	MTCMOS SCCMOS BGMOS
Variable V_{TH}	VTCMOS	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	(SCCMOS) (BGMOS)
Variable V_{DD}	Variable Supply	

Multi-Threshold CMOS (MTCMOS)



Benefits

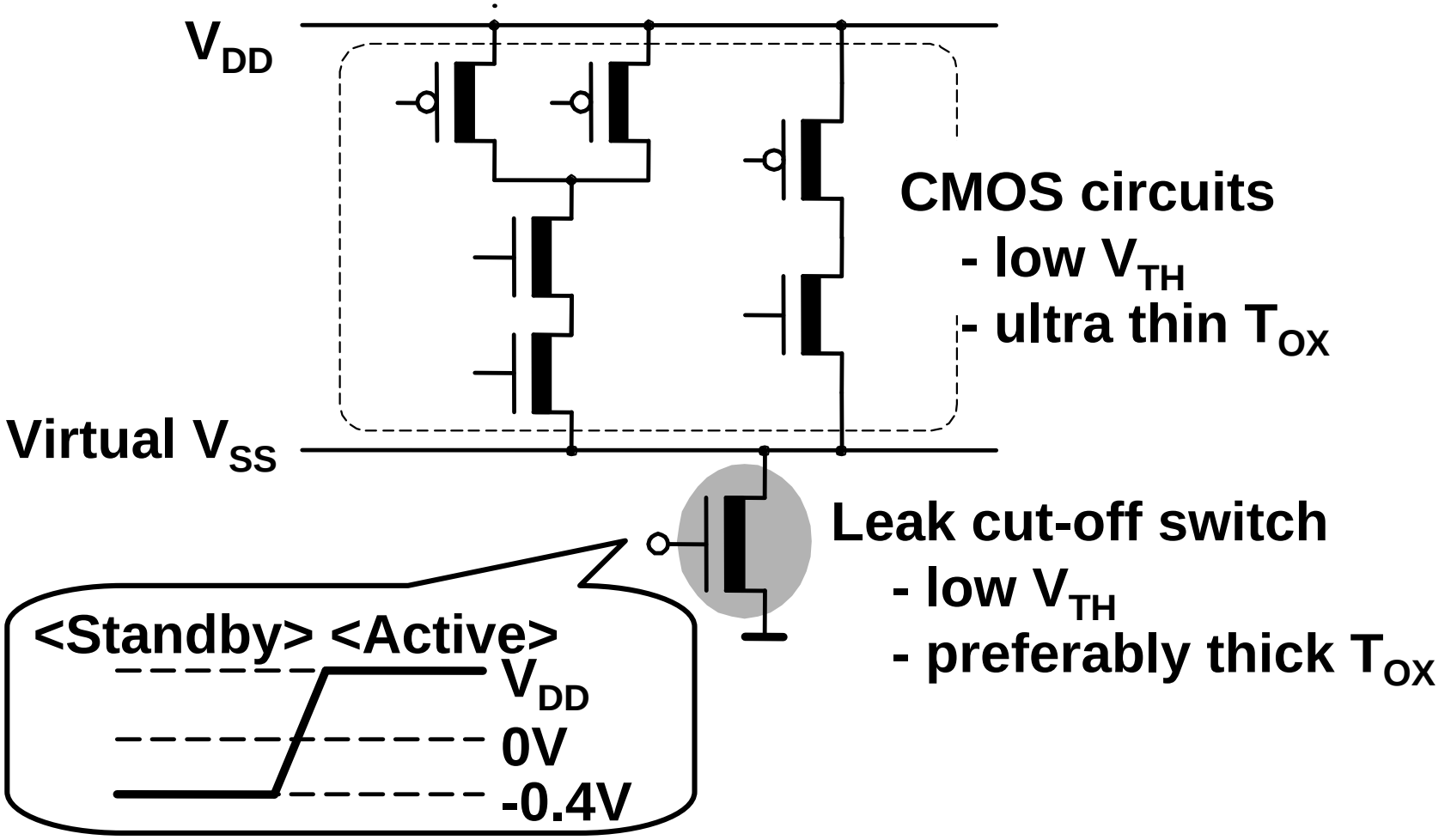
- **Low leakage current in standby**

→ **Reduced by 3 or 4 orders of magnitude.**

Issues

- **Large leak cut-off transistor**
- **Difficult for ultra low voltage**
- **Need for special Flip Flop**

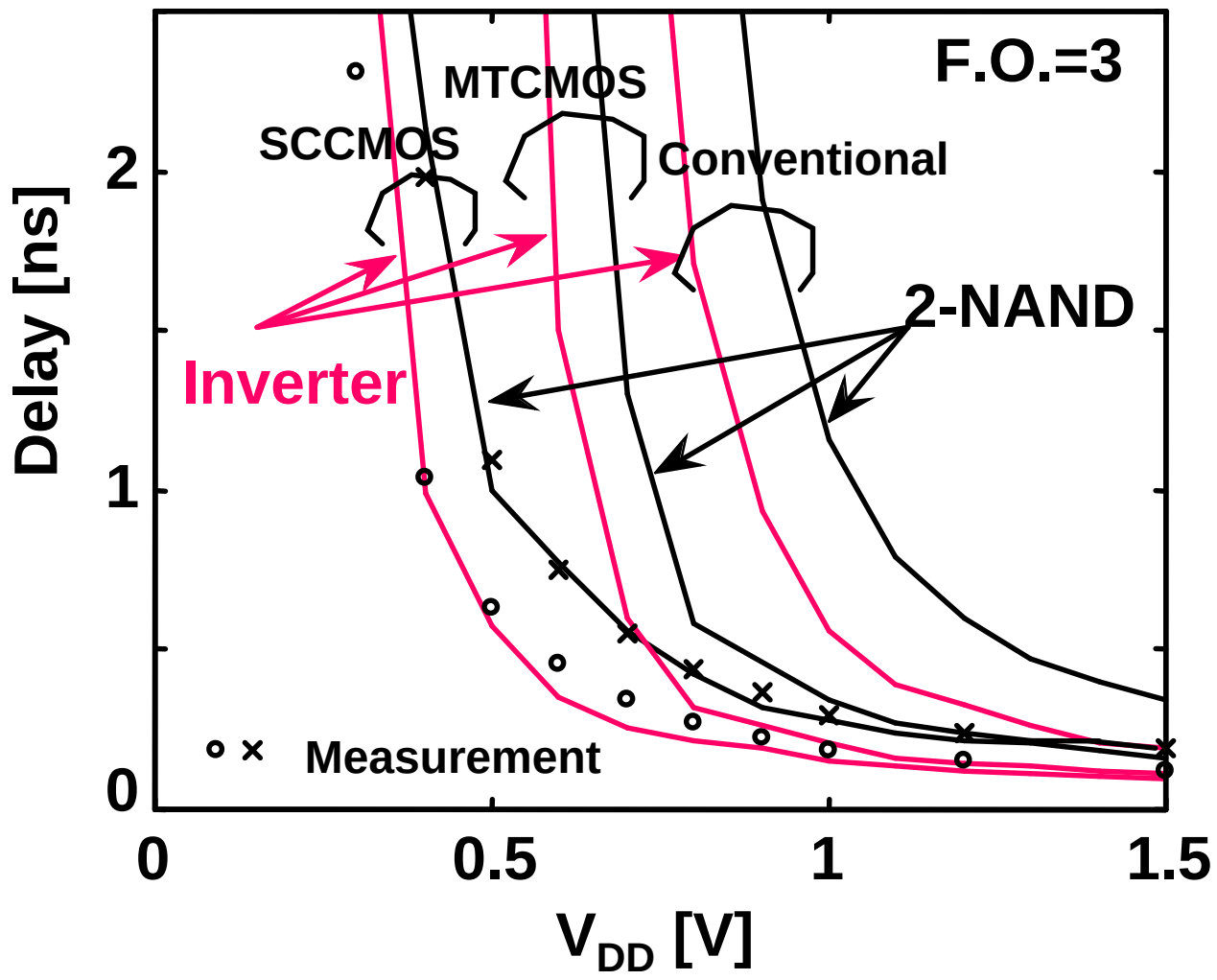
Super Cut-Off CMOS (SCCMOS)



V_{DD} can be decreased to 0.5V

V_{TH} can be decreased to less than 0.2V

Delay characteristics



SCCMOS
0.2V V_{TH} circuit with 0.2V V_{TH} cut-off MOSFET

MTCMOS
0.2V V_{TH} circuit with 0.6V V_{TH} cut-off MOSFET

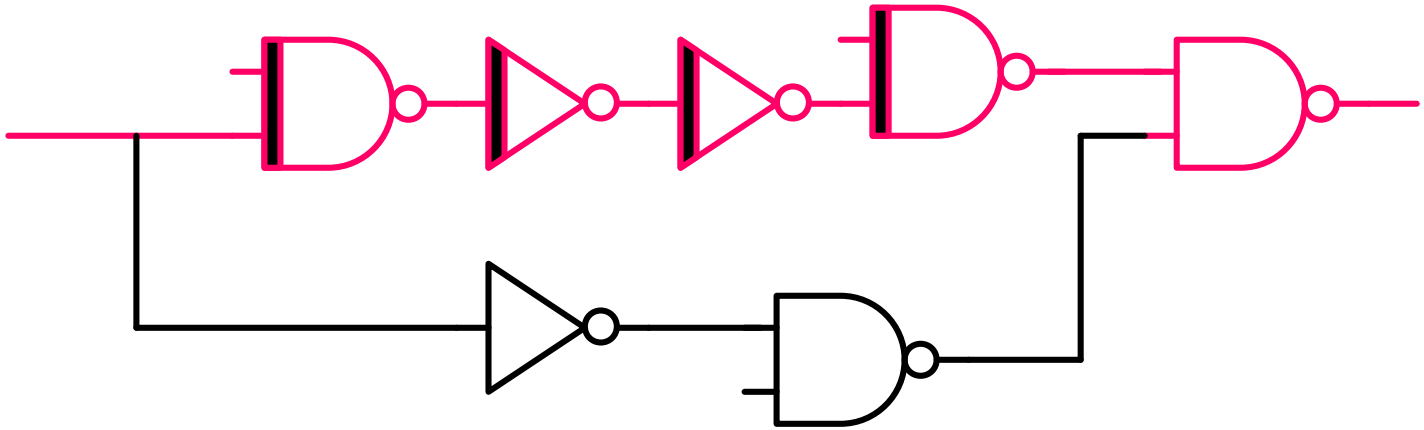
Conventional
All 0.6V circuit No cut-off MOSFET

Standby current = 1pA

Controlling V_{DD} and V_{TH} for low power

	Active Power	Standby Power
Multiple V_{TH}	Dual-V_{TH}	MTCMOS SCCMOS BGMOS
Variable V_{TH}	VTCMOS	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	(SCCMOS) (BGMOS)
Variable V_{DD}	Variable Supply	

Dual-Threshold Voltage technique



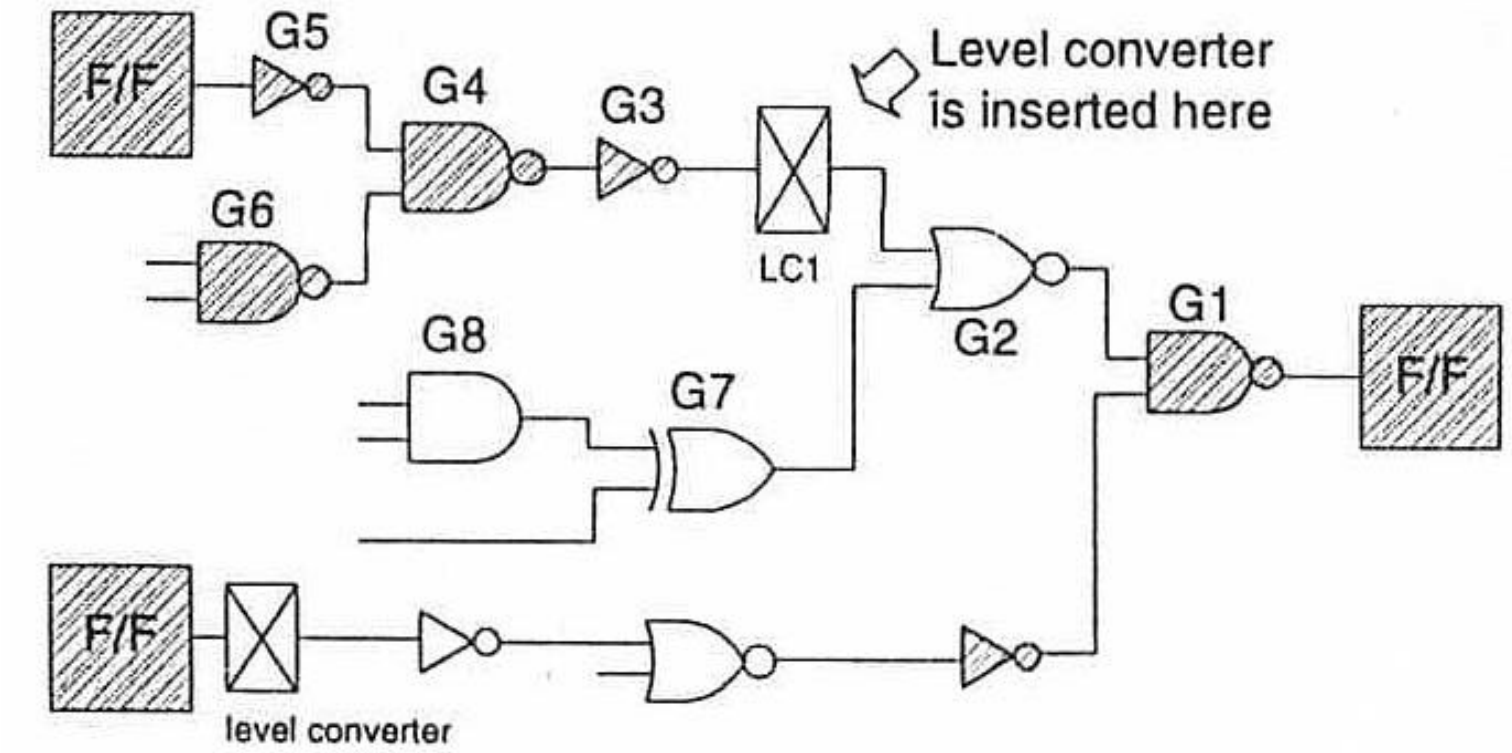
— **Critical paths ® Low-V_{TH} MOS**
® High leakage, High speed

— **Non-critical paths ® High-V_{TH} MOS**
® Low leakage, Low speed

Controlling V_{DD} and V_{TH} for low power

	Active Power	Standby Power
Multiple V_{TH}	Dual-V_{TH}	MTCMOS SCCMOS BGMOS
Variable V_{TH}	VTCMOS	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	(SCCMOS) (BGMOS)
Variable V_{DD}	Variable Supply	

Dual Supply Voltage scheme



Critical paths ® High-V_{DD} ® High speed

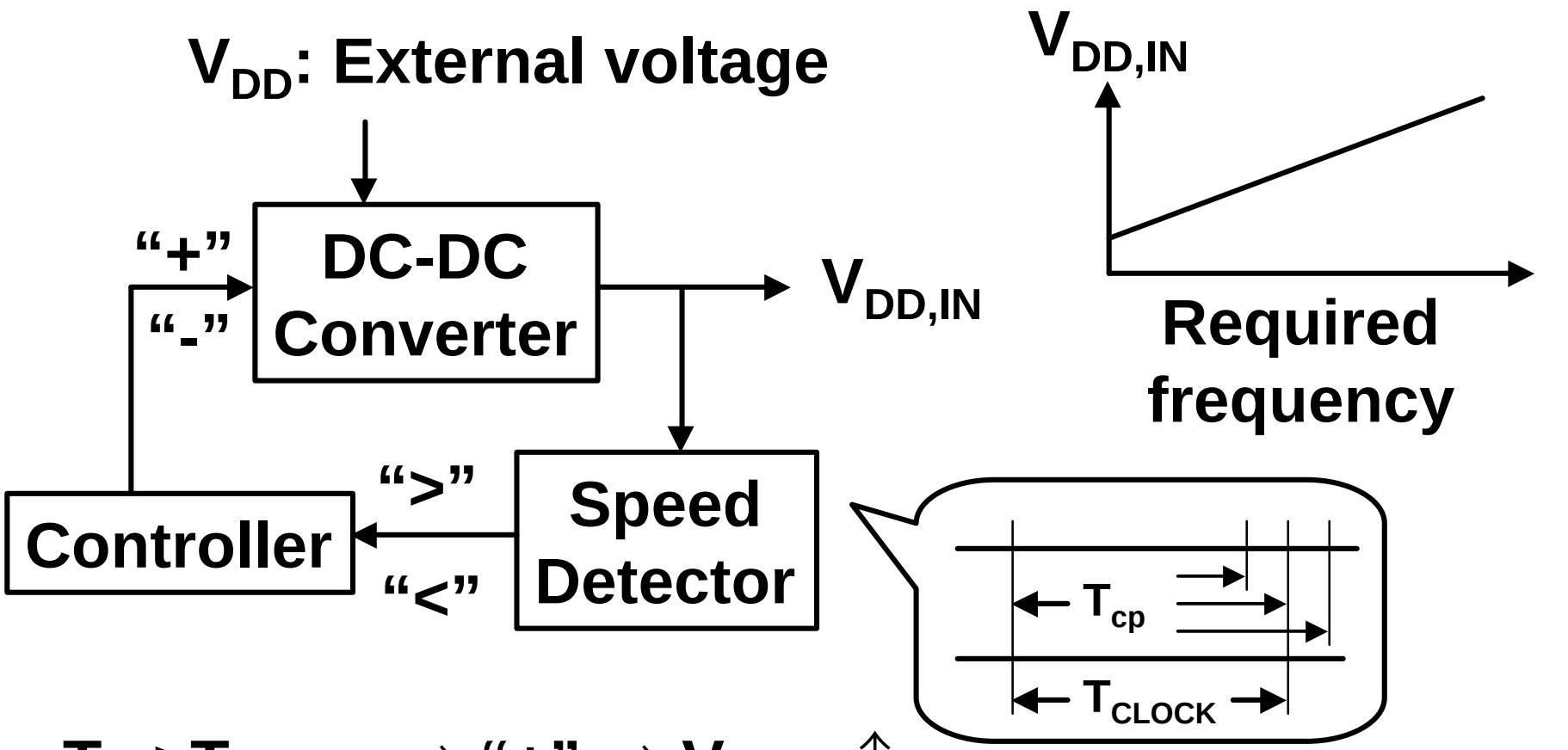
Non-critical paths ® Low-V_{DD} ® Low power

Needs high speed level converter.

Controlling V_{DD} and V_{TH} for low power

	Active Power	Standby Power
Multiple V_{TH}	Dual-V_{TH}	MTCMOS SCCMOS BGMOS
Variable V_{TH}	VTCMOS	VTCMOS
Multiple V_{DD}	Dual-V_{DD}	(SCCMOS) (BGMOS)
Variable V_{DD}	Variable Supply	

Variable Supply Voltage scheme (VS)



- $T_{cp} > T_{CLOCK} \rightarrow$ "+" $\rightarrow V_{DD,IN} \uparrow$
- $T_{cp} = T_{CLOCK} \rightarrow$ No change
- $T_{cp} < T_{CLOCK} \rightarrow$ "-" $\rightarrow V_{DD,IN} \downarrow$

T_{cp}: Delay time of critical path

T_{CLOCK}: Clock cycle

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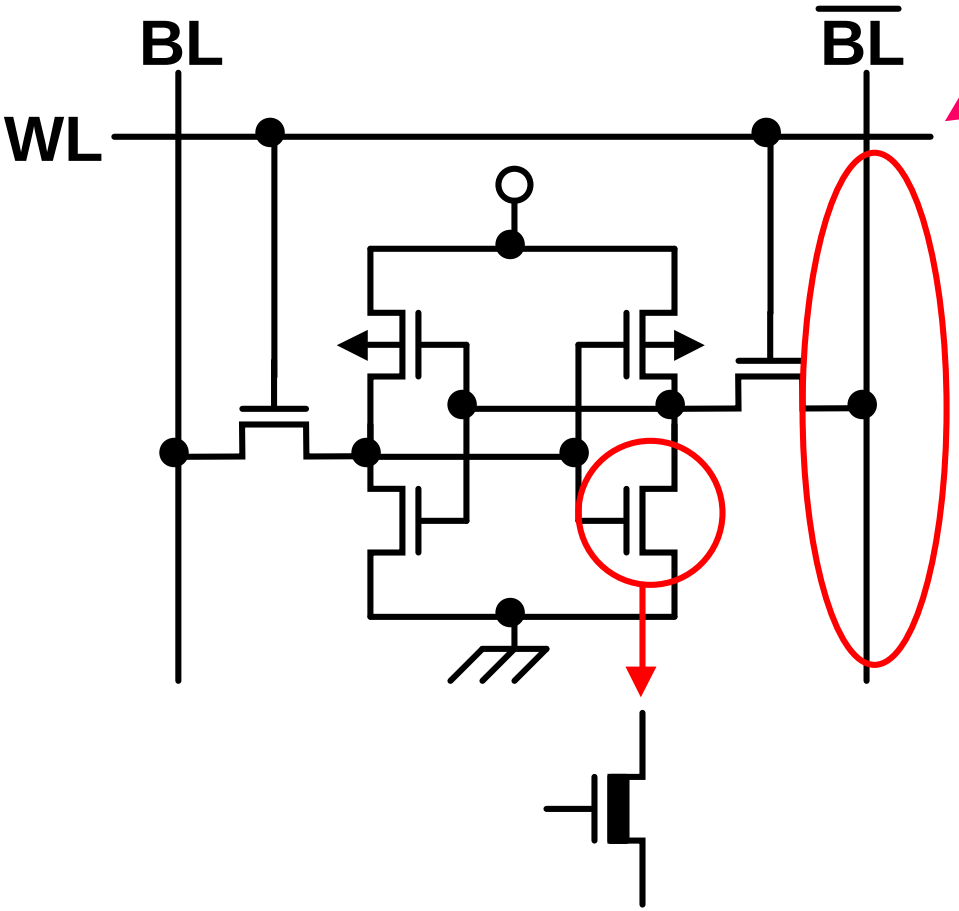
Low voltage SRAM memory cells

Lowering V_{DD} of SRAM cell is difficult.

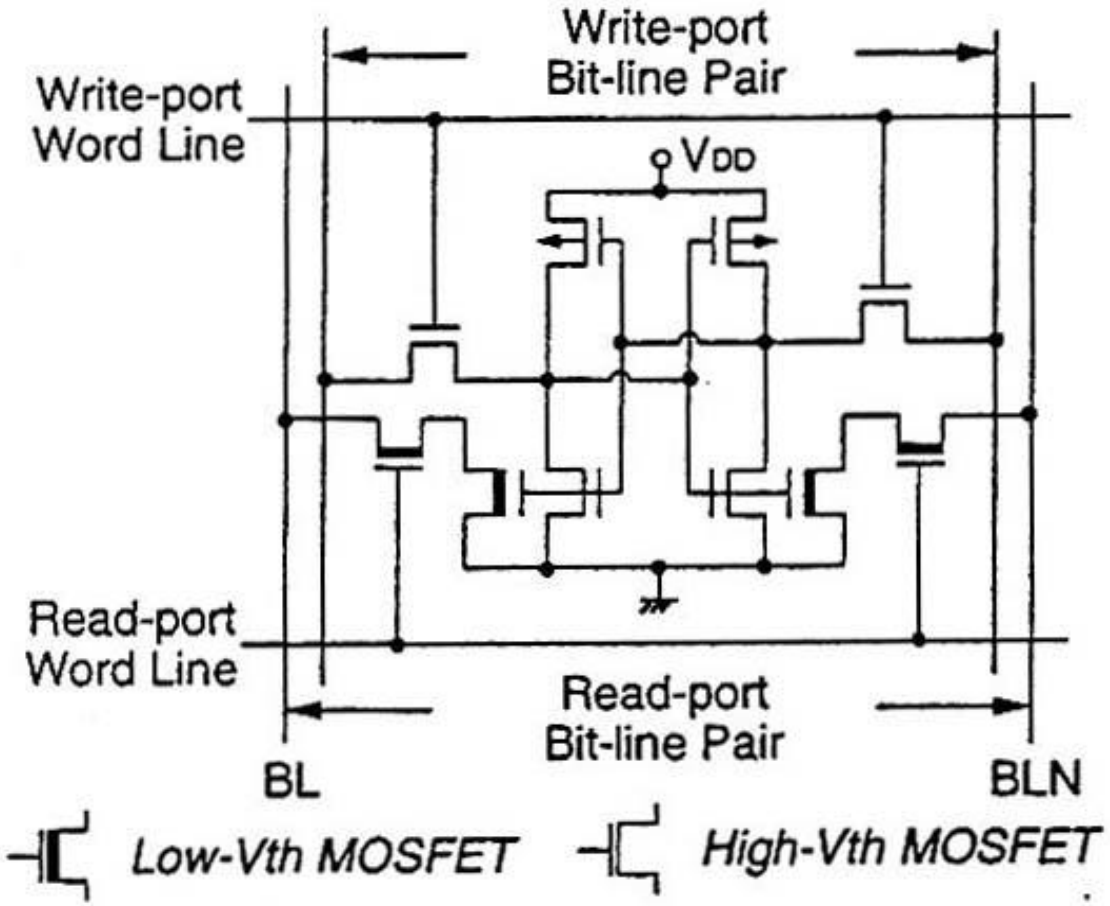


Long wire

Large capacitance → Needs strong current supply.

Leak → Data will be lost.

0.5-1V V_{DD} SRAM



V_{DD}=0.5V
High-V_{TH}=0.35V
Low-V_{TH}=0.15V

- Write-port and Read-port are divided in order to cut read error.
- Precharge level of Bit line is low because of leakage at low-V_{TH} MOS.

Low precharge → Low speed
High-V_{TH}=0.35V → Low reliability

Summary

Low power technologies will be most important technologies for future VLSI processor.

- **Low voltage logic technologies**

	Active Power	Standby Power
Multiple V_{TH}	Dual-V_{TH}	MTCMOS, SCCMOS
Variable V_{TH}		
Multiple V_{DD}	Dual-V_{DD}	(SCCMOS)
Variable V_{DD}	Variable Supply	

- **Low voltage SRAM memory cell**

Future VLSI processor