Low-Power SRAM Design using Low-Voltage and Low-Swing Techniques

Master thesis presentation
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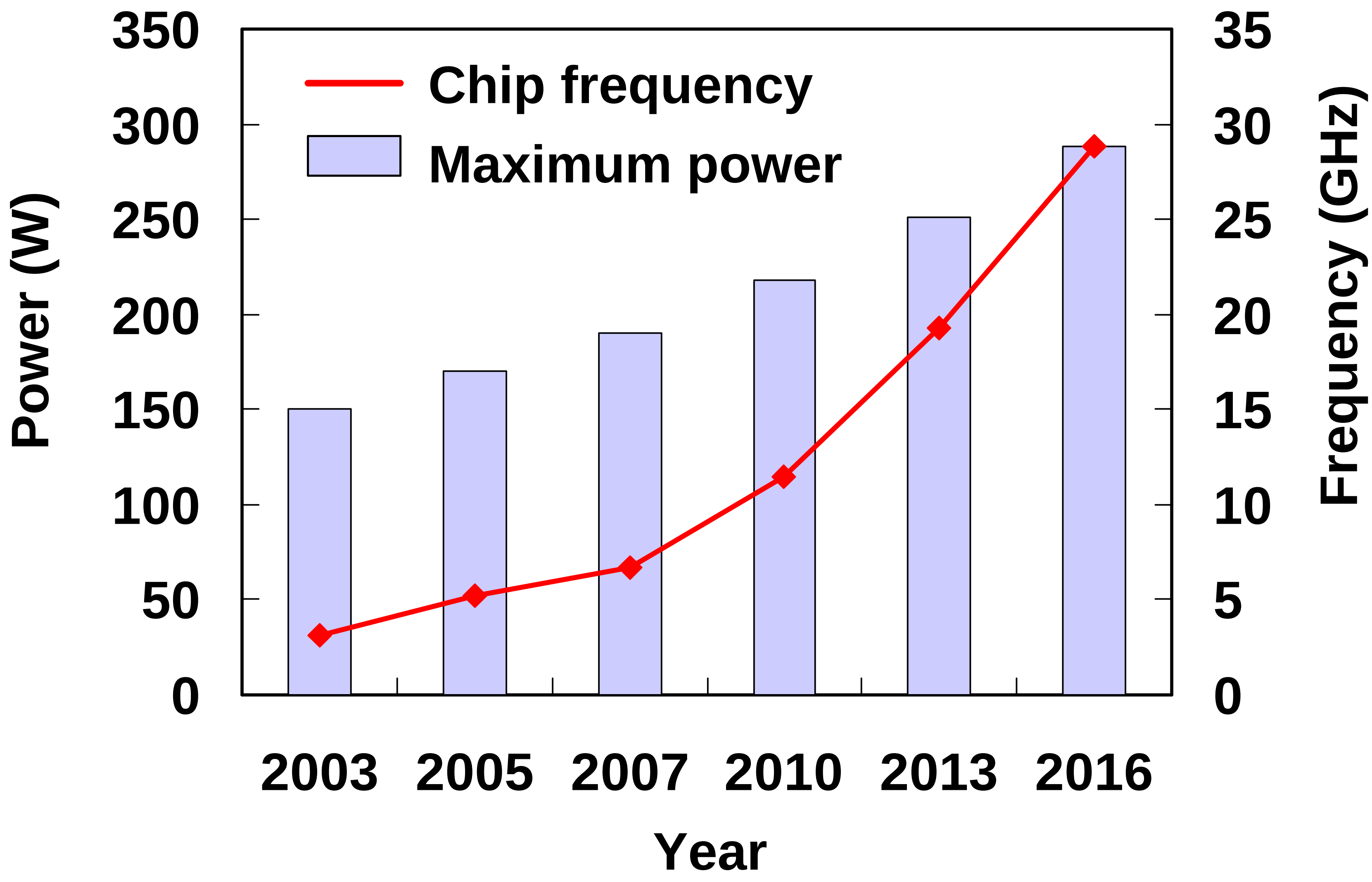
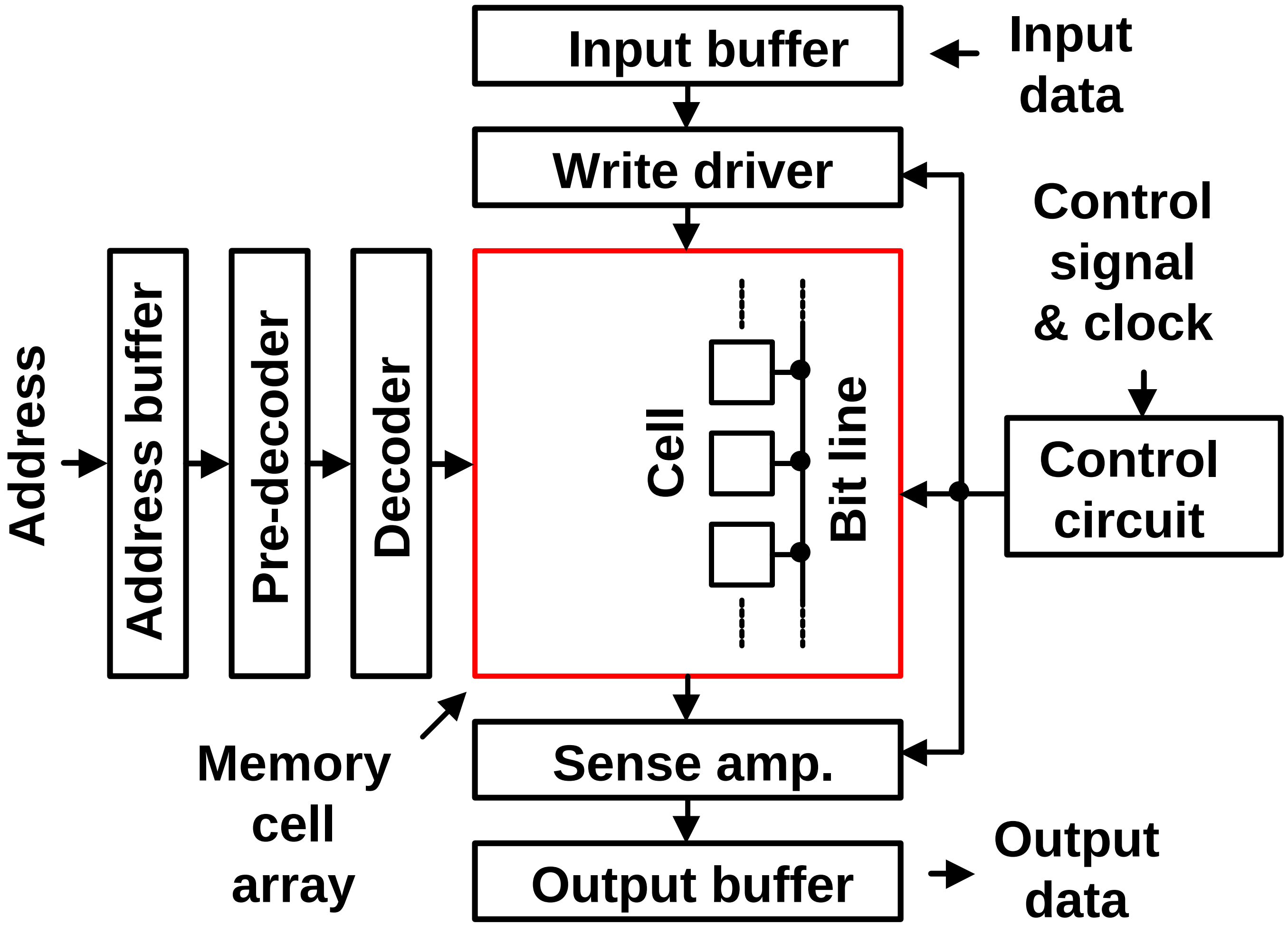
Contents

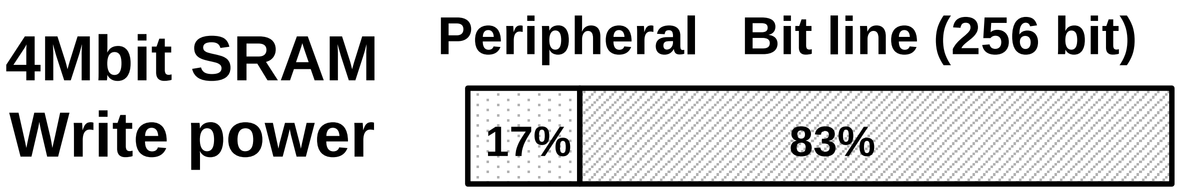
Power crisis in VLSI



(ITRS: International Technology Roadmap for Semiconductors 2001)

SRAM Architecture





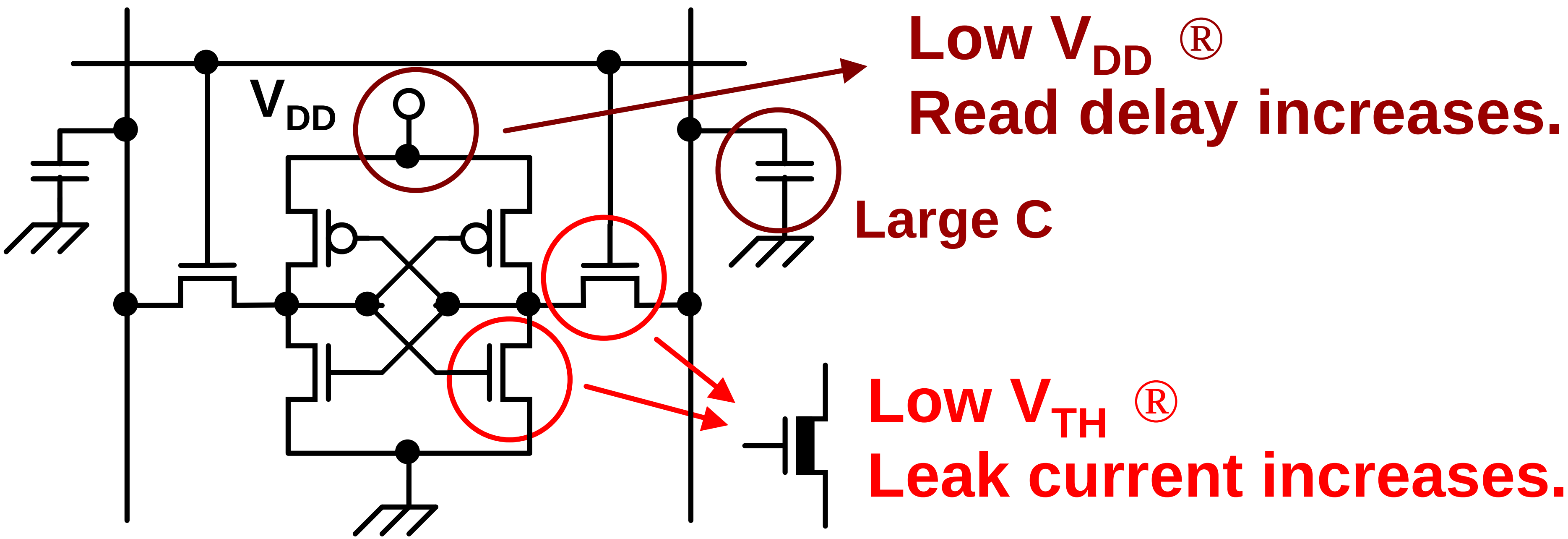
Low voltage SRAM

$P = f_{CLK} C_L V_{DD}^2$

f_{CLK} : clock frequency C_L : load capacitance
V_{DD} : supply voltage

Lowering V_{DD} is the best solution to power reduction in logic circuits.

Lowering V_{DD} of SRAM cell is difficult.



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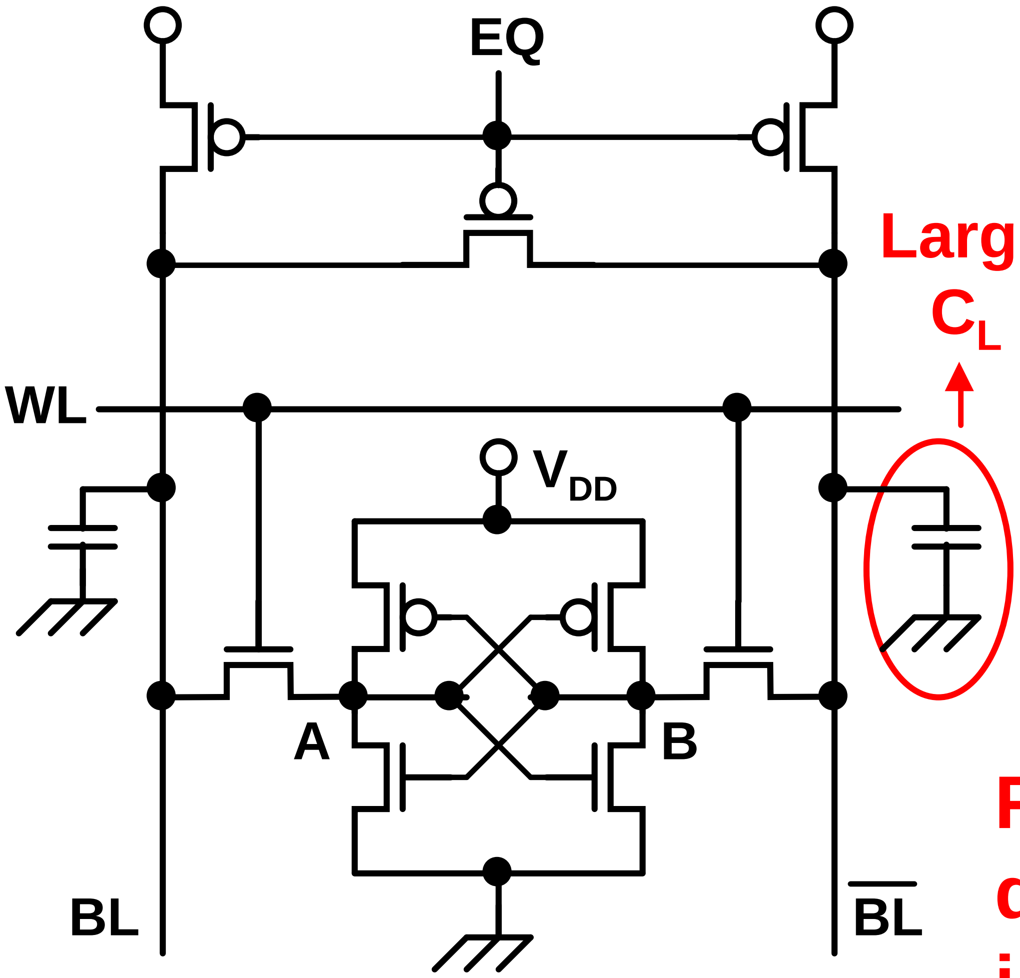
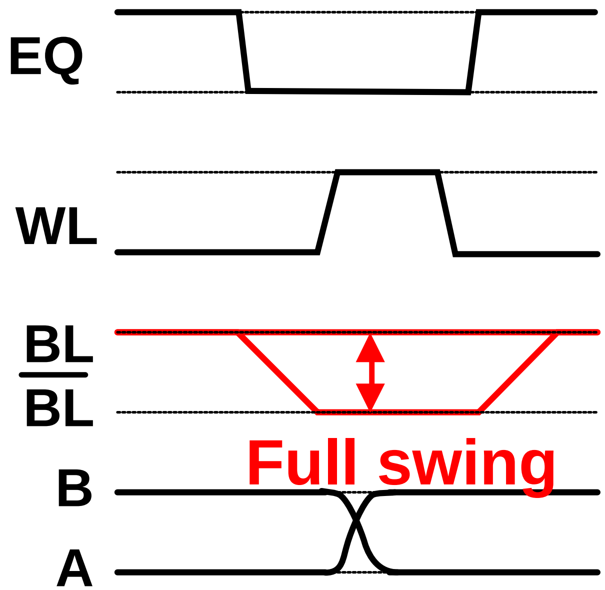
1. Background
2. Write power saving scheme
3. Power saving scheme for peripheral circuits and decoders
4. Power saving scheme for register file
5. Conclusion

Conventional SRAM



$$P = f_{CLK} C_L V_{DD}^2$$

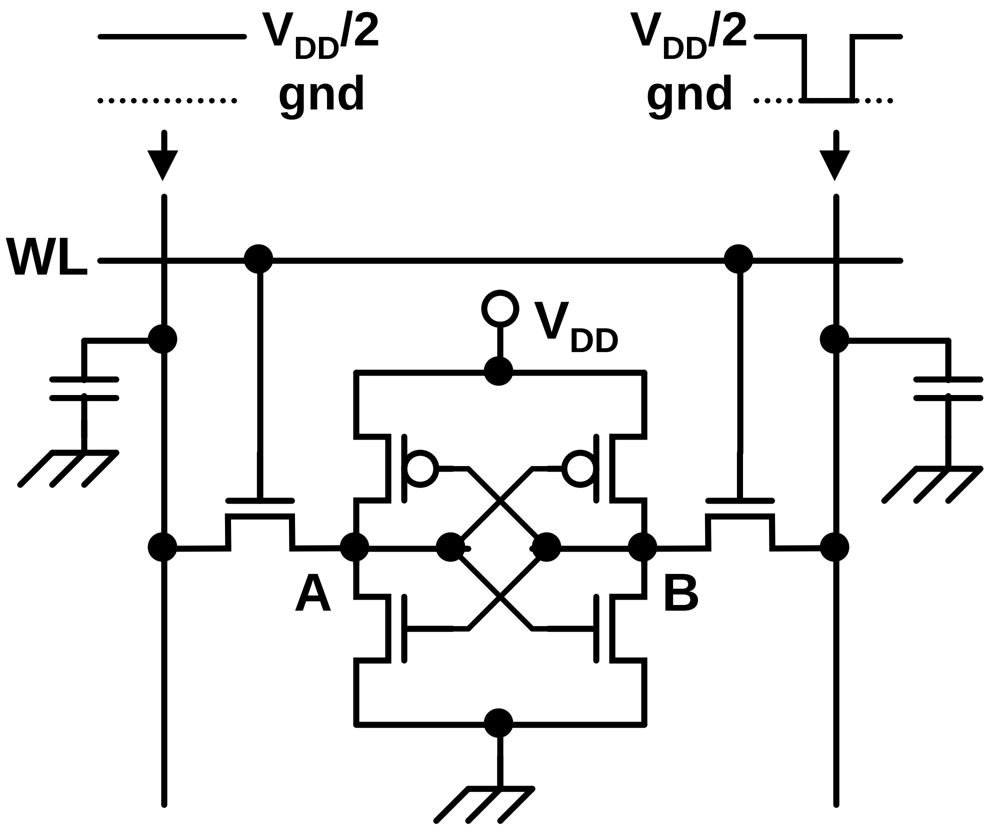


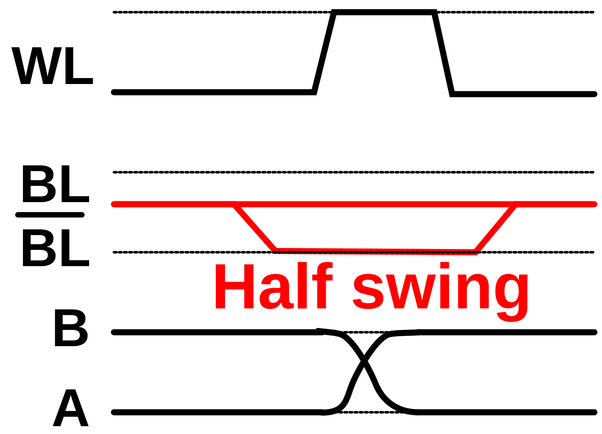
Write cycle waveforms

Full swing of bit-line dissipates large power in write cycles.

® dominant

SRAM cell using half-swing bit-line



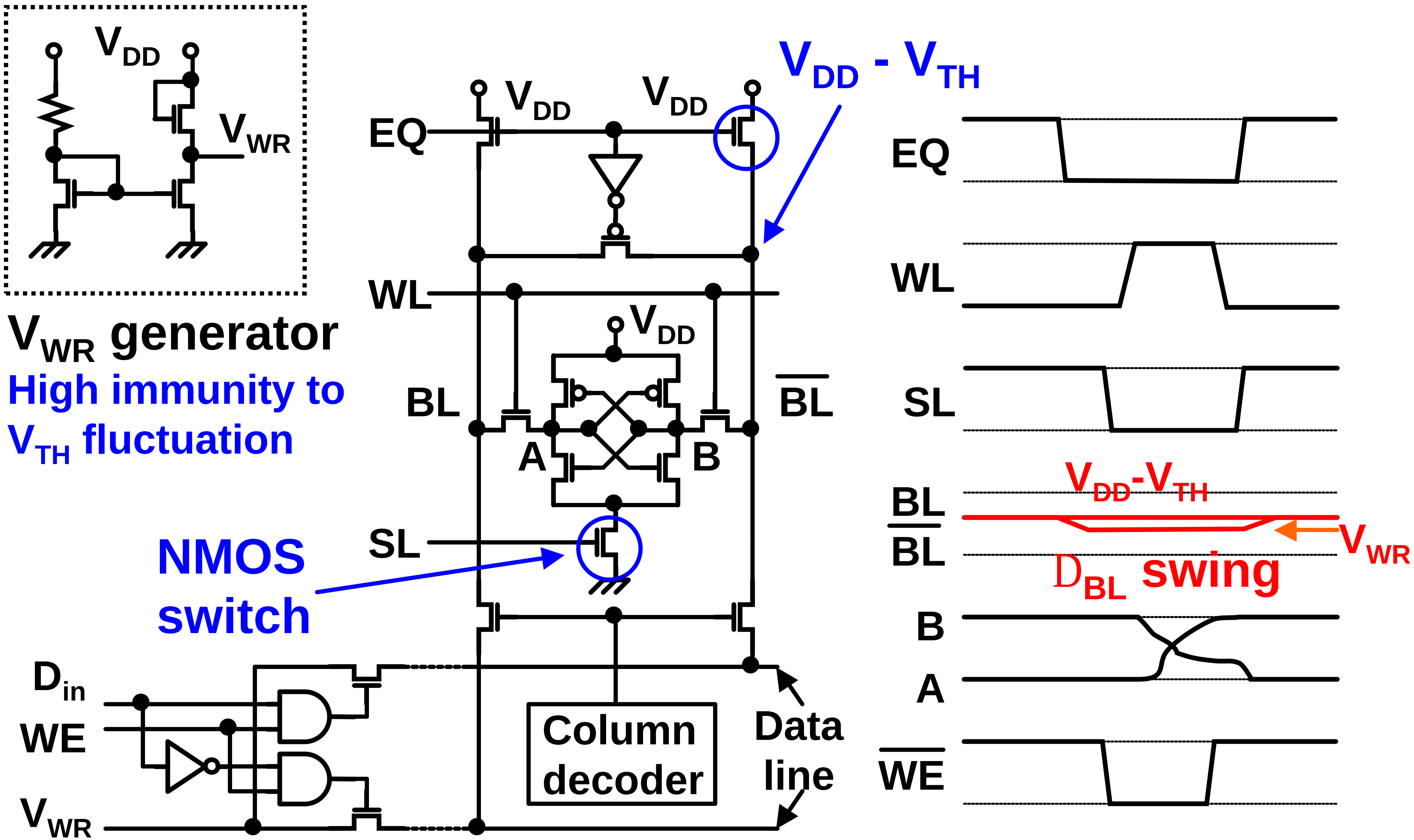


$P = f_{CLK} C_L (1/4) V_{DD}^2$
with charge recycling

- **Further power reduction is difficult because cell node potential cannot be inverted at lower swing.**
- **Additional power in alternate write and read cycles.**

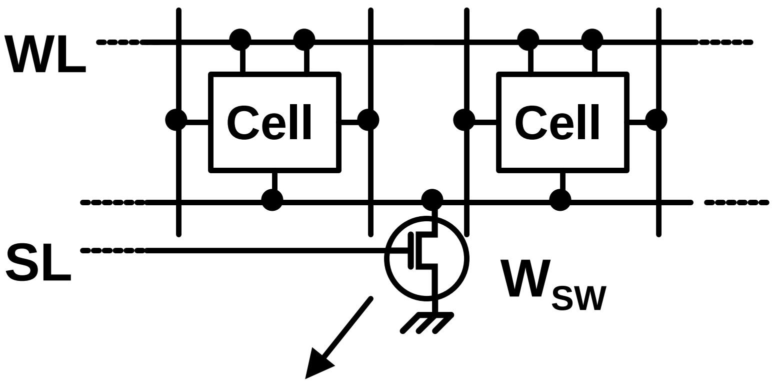
(Mark A. Horowitz et al.,
"Low-power SRAM Design Using Half-Swing Pulse-mode Techniques",
IEEE Journal of SSC, Vol. 33, pp. 1659-1671, Nov., 1998)

Sense-amplifying cell (SAC) scheme

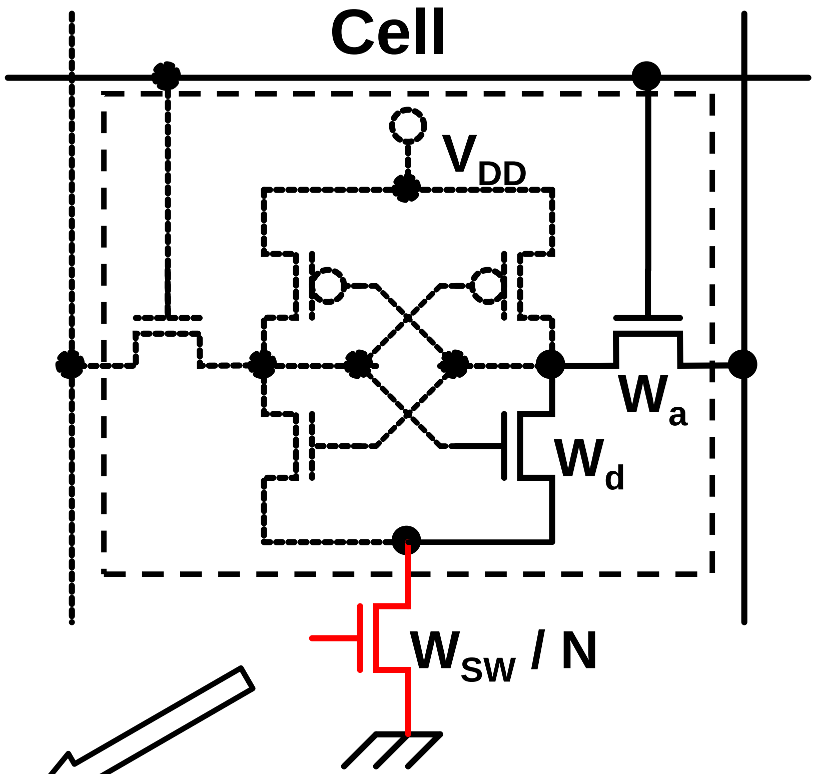


$$P = f_{CLK} C_L \Delta V_{BL}^2$$

Design Considerations



NMOS switch is shared by N cells (N= 2, 4, 8)

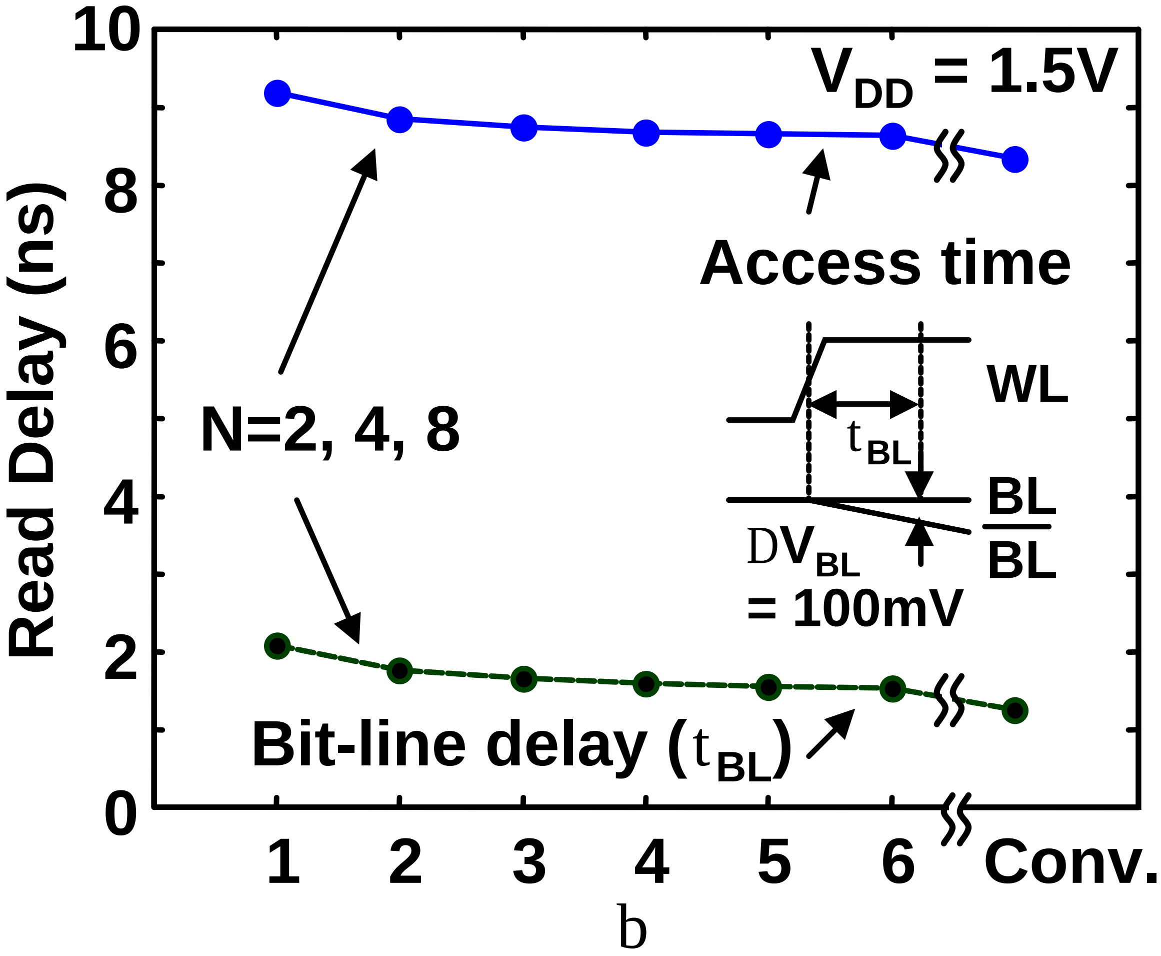


- **Read access time** -
- **Noise margin** —
- **Area overhead** -

b = W_{SW} / N / W_a

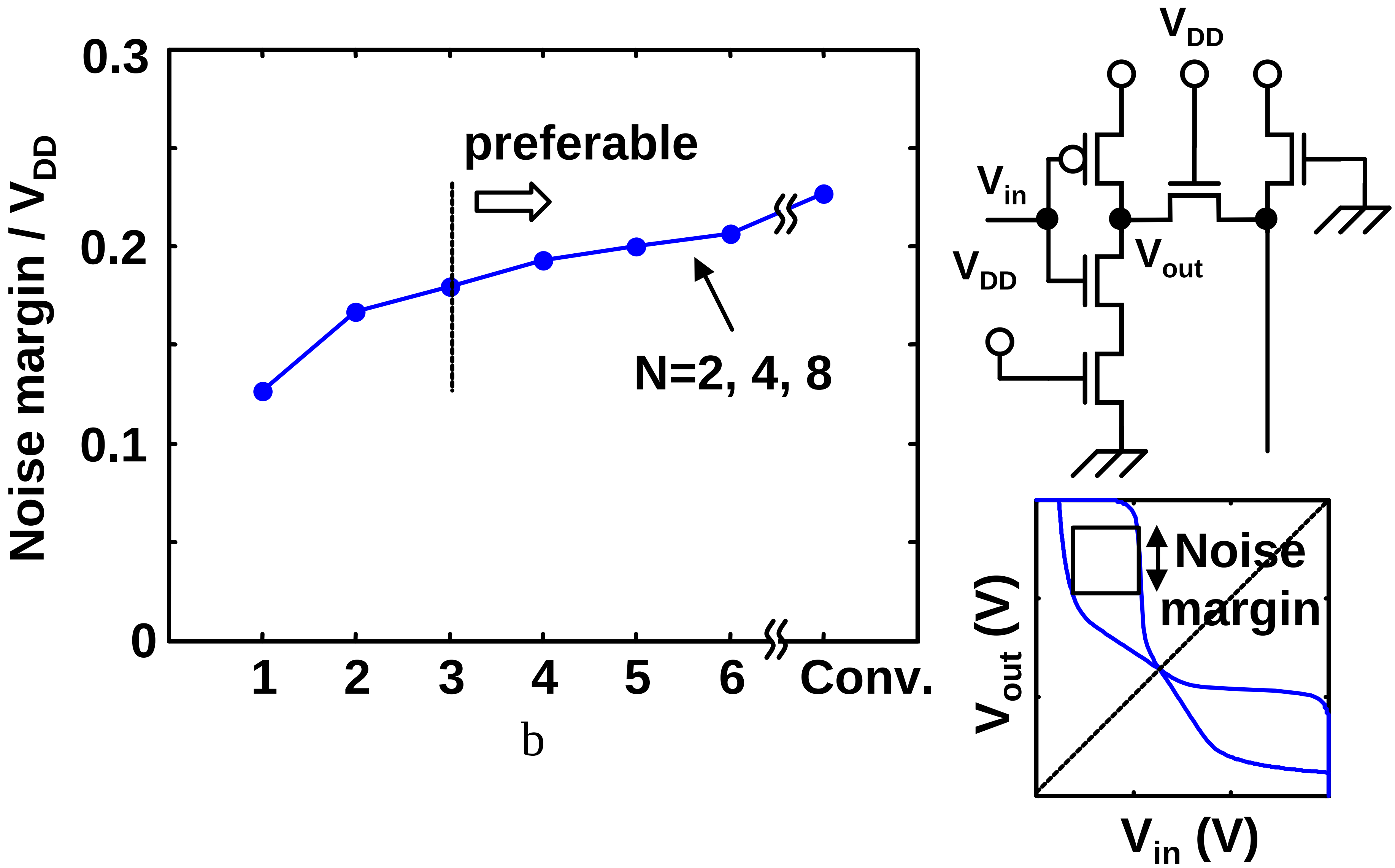
$W_d = 3W_a$

Read delay

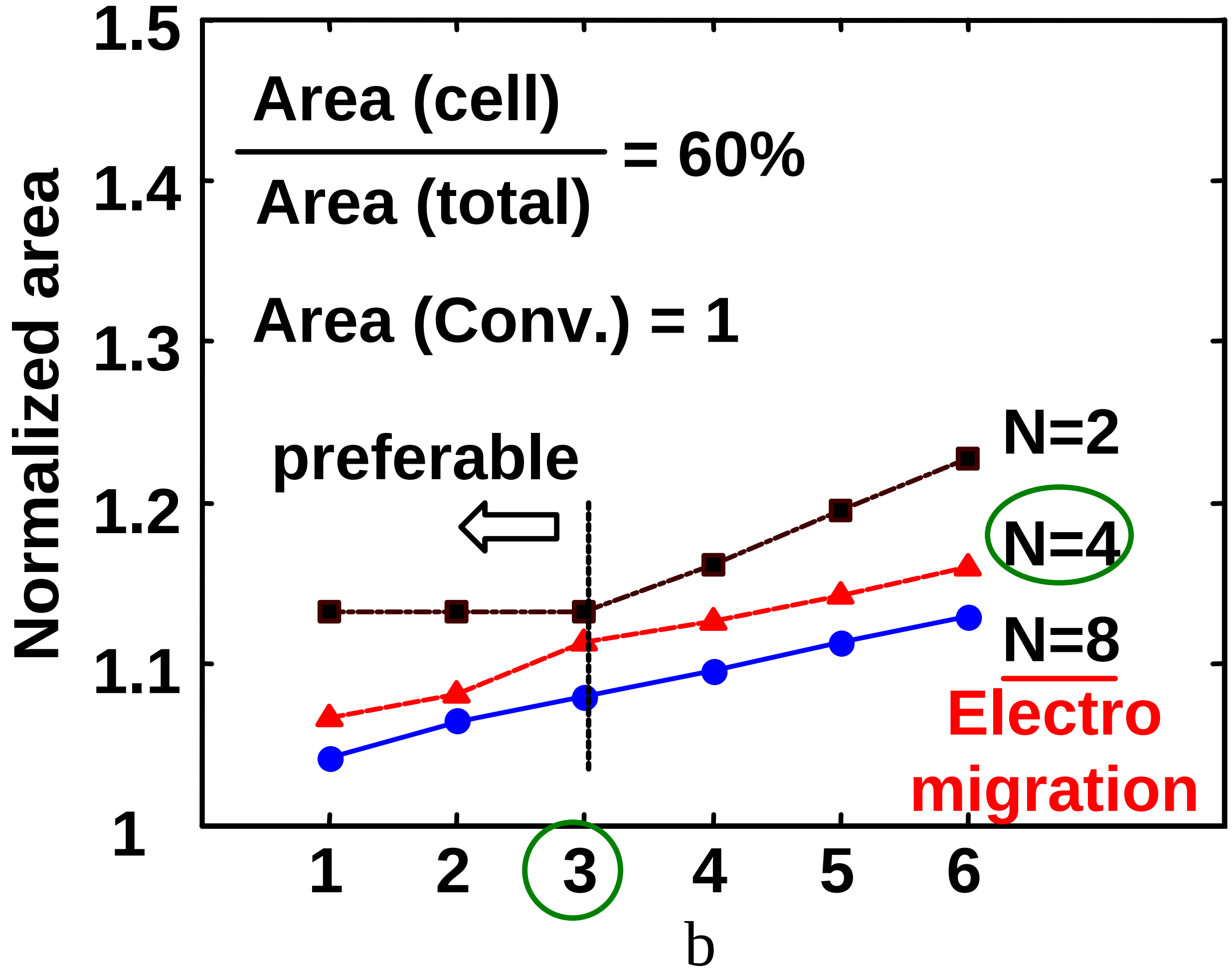


Addressing time: 4.0 ns (calculated)
Data output time: 3.1 ns (calculated)

Noise margin analysis



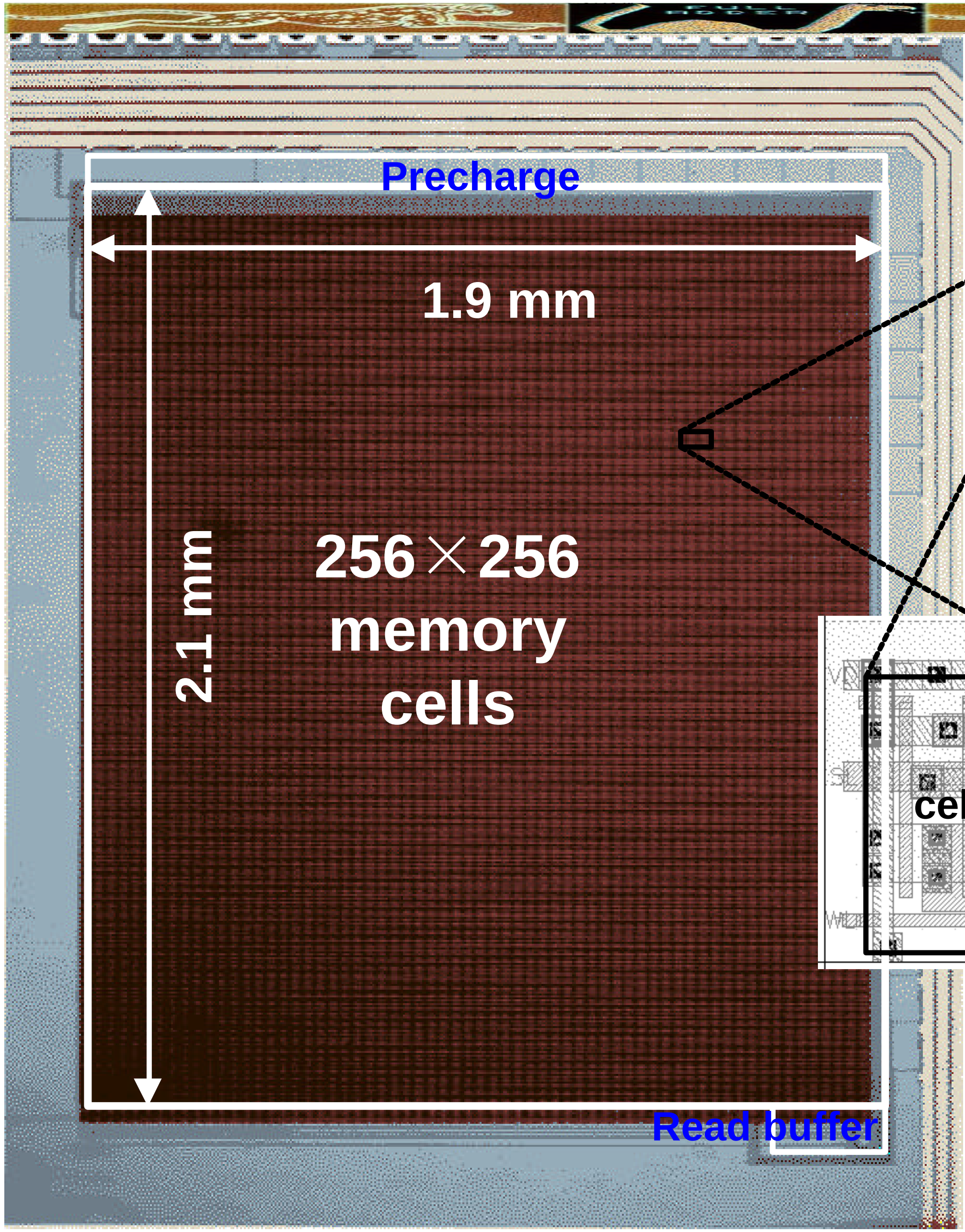
Area overhead



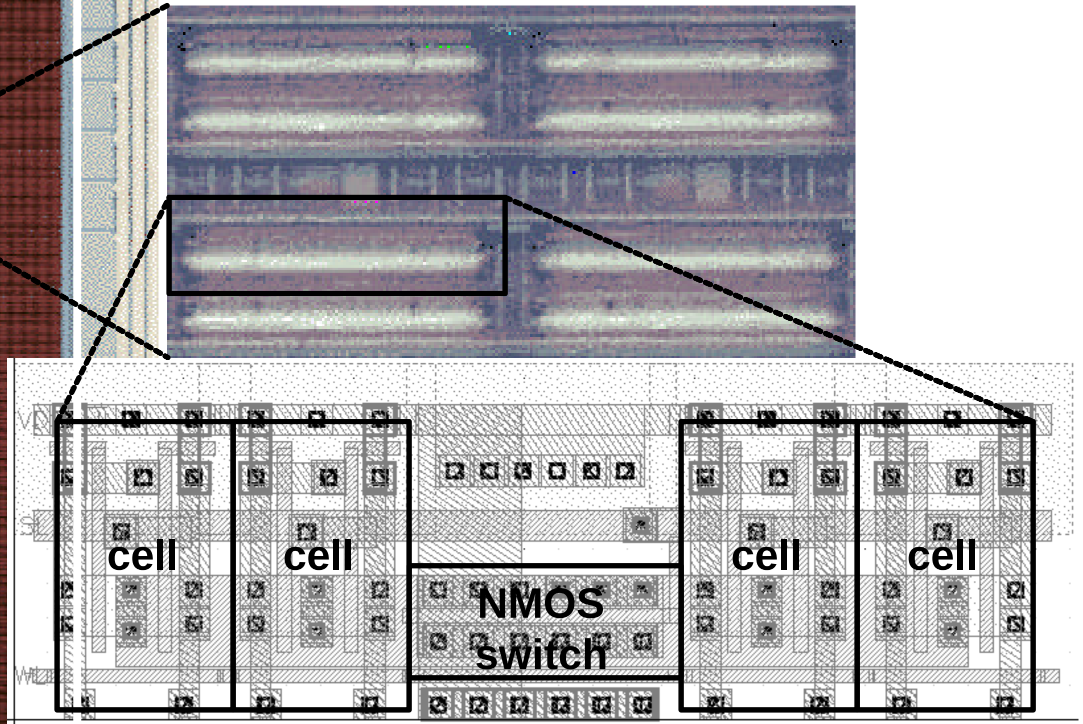
b=3, N=4

- Read access time: 5% -
- Noise margin: $0.05V_{DD}$ -
- Area overhead: 11% -

Microphotograph of 1st SRAM test chip



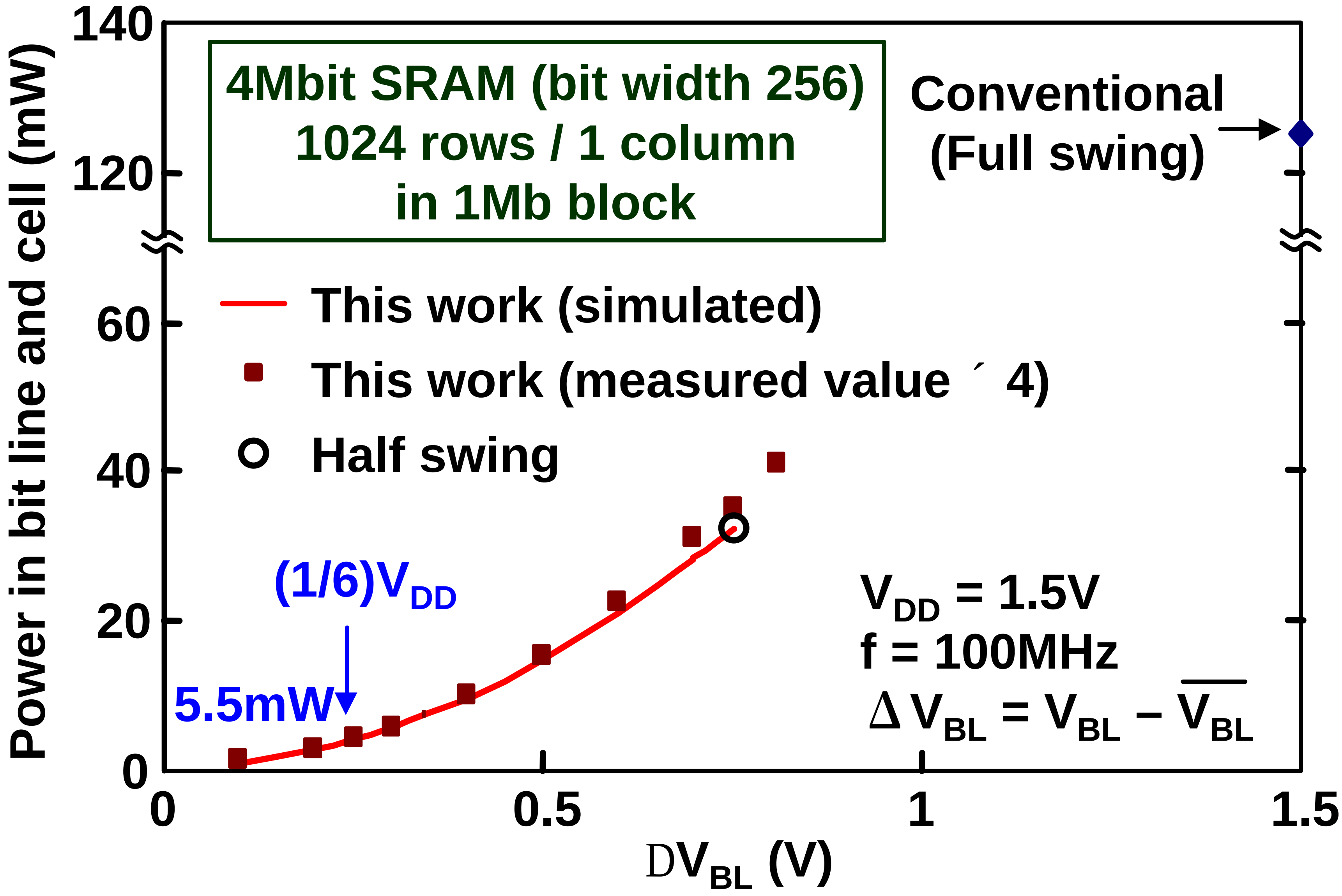
Technology:
0.35-mm CMOS 3-metal (Rohm)



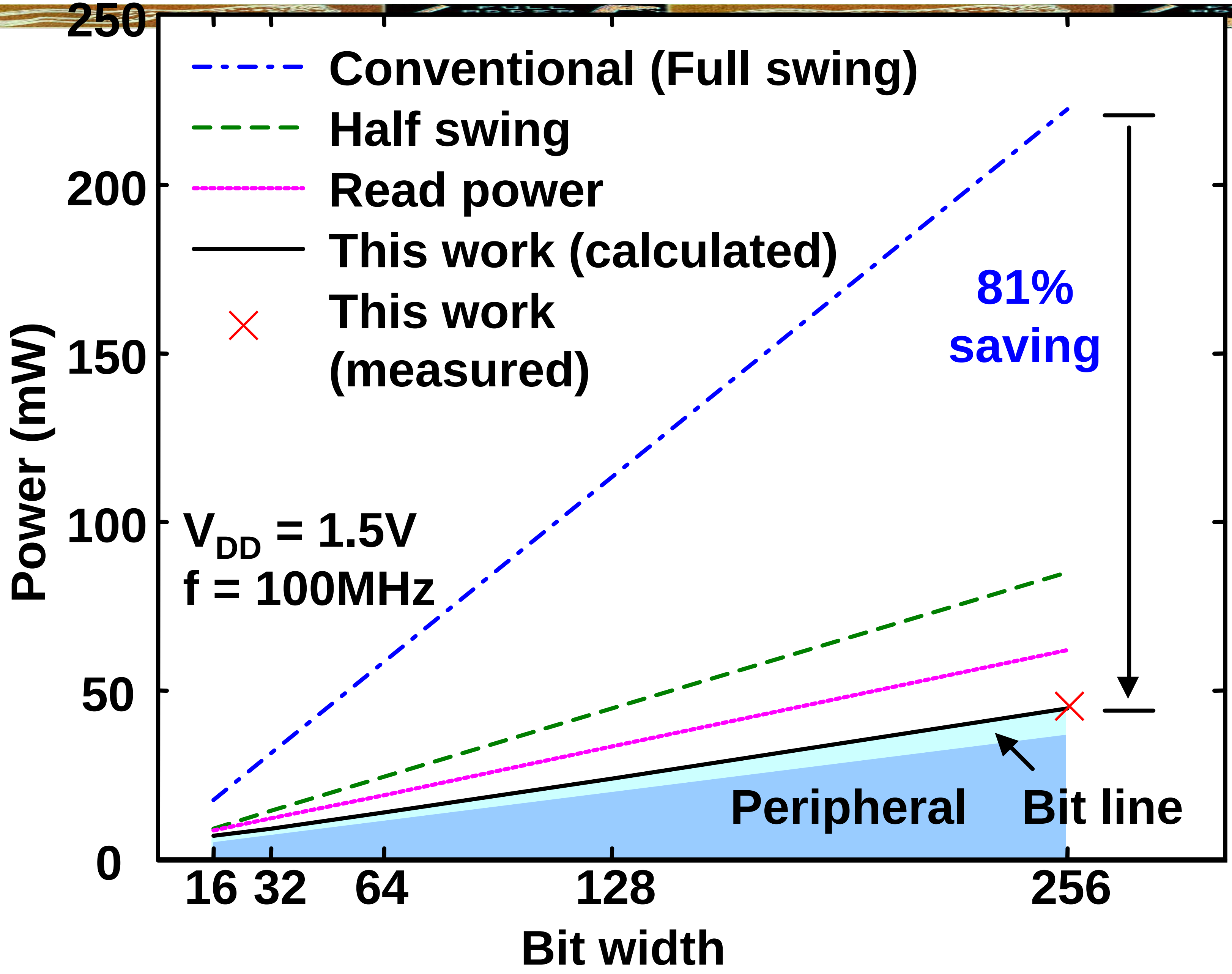
Area overhead 21% -

$$\left(\frac{\text{Area (cell)}}{\text{Area (total)}} = 60\% \right)$$

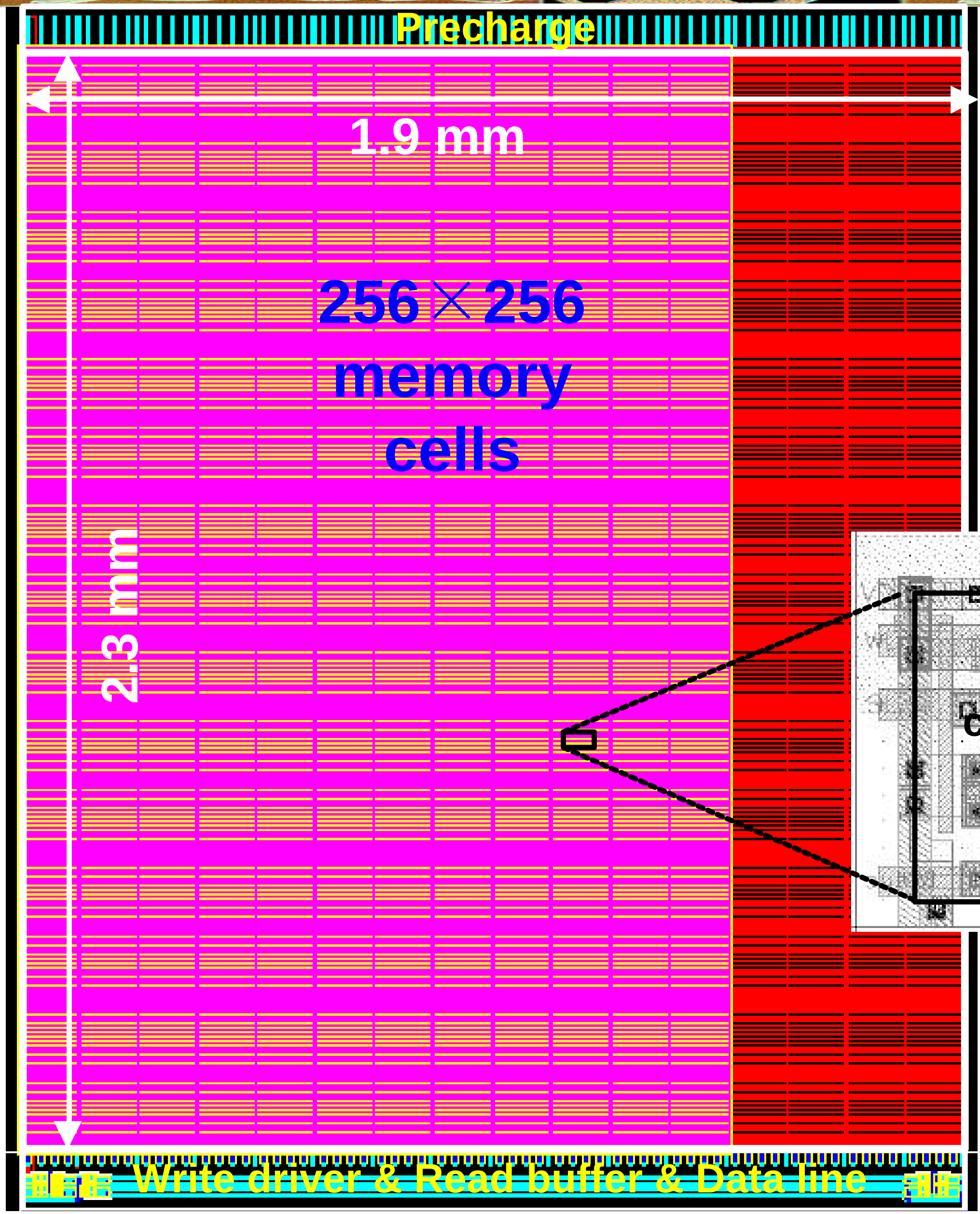
Write power consumption in memory cell arrays



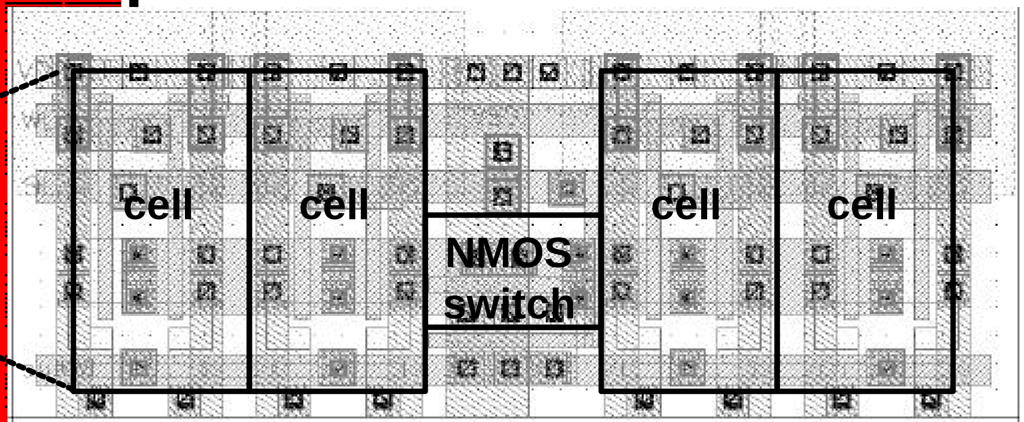
Total write power consumption of 4Mbit SRAM



Layout of 2nd SRAM test chip



Technology:
0.35-μm CMOS 3-metal
(Rohm)



Area overhead 11%-

$$\left(\frac{\text{Area (cell)}}{\text{Area (total)}} = 60\% \right)$$

Summary of SAC scheme

- **Sense-amplifying cell (SAC) scheme saves total write power of 4Mbit SRAM by 81% at bit width of 256.**

- **Test chip is fabricated at b=3, N=4.**

- **Read access time increases by 5%.**
- **Noise margin increases by 0.05V_{DD}.**
- **Total area increases by 11%.**

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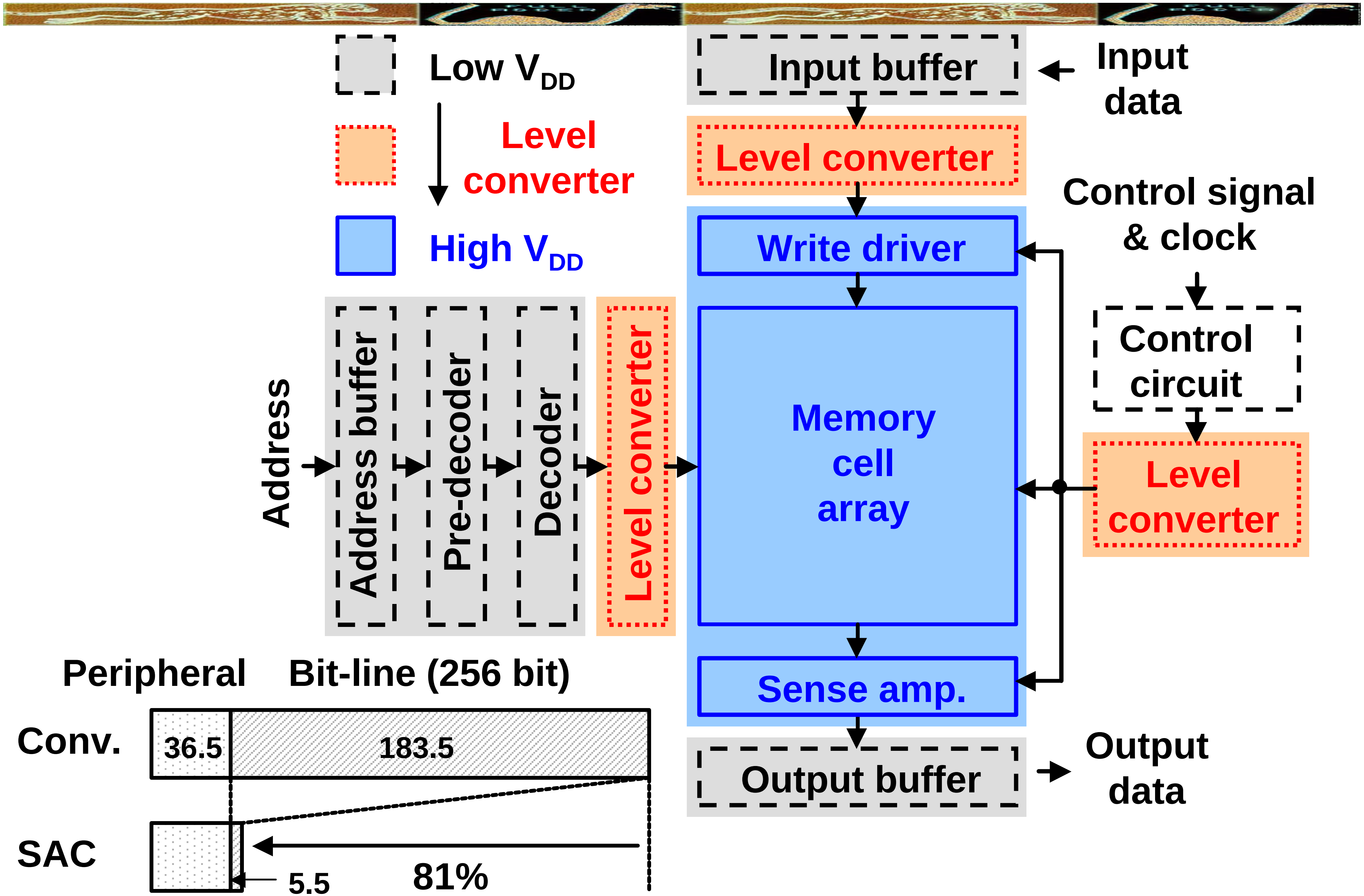
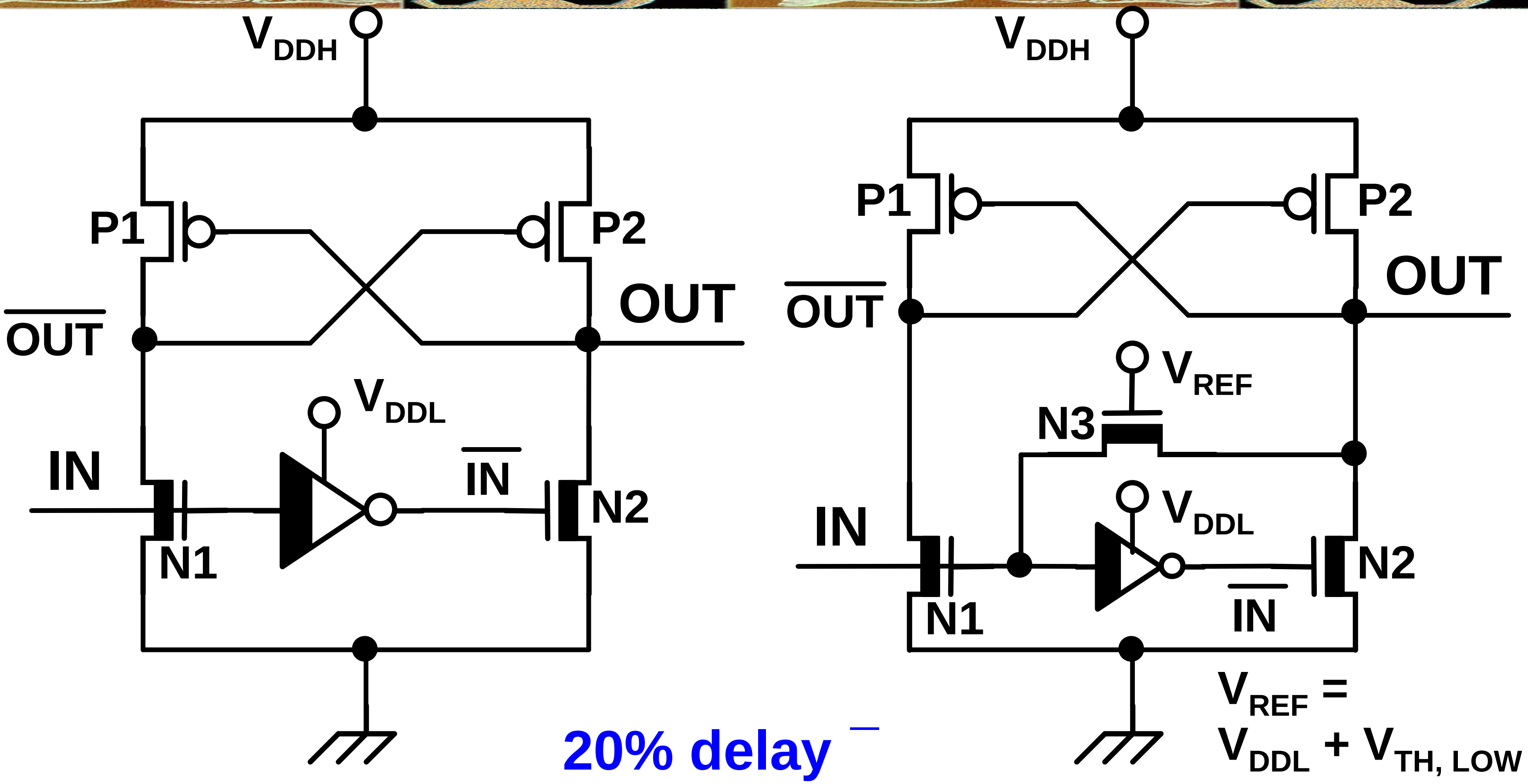
Dual-V_{DD} SRAM architecture



Conventional and proposed converter

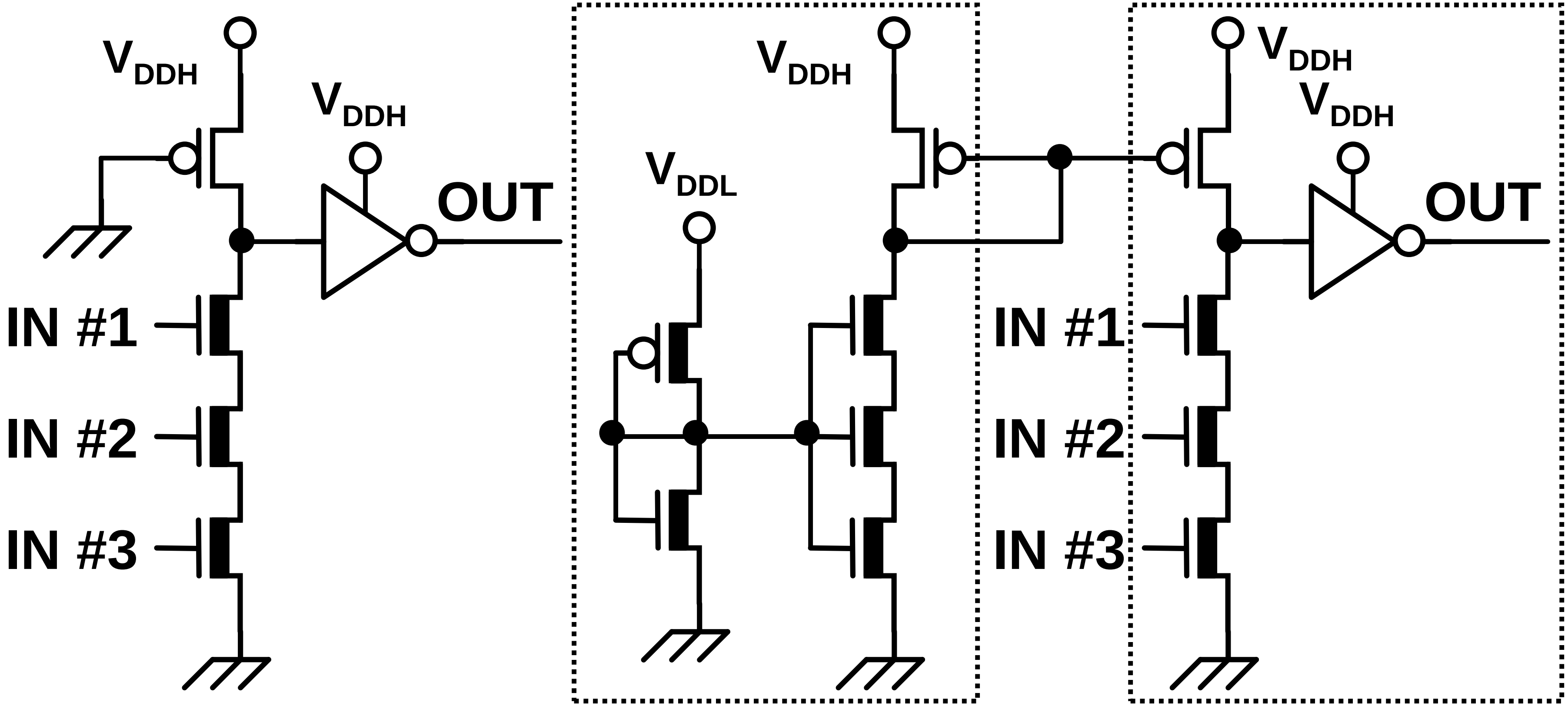


20% delay ⁻

Conventional ⟹ Proposed bypass level converter (BLC)

Low immunity to V_{TH} fluctuation

Proposed level converter



Pseudo NMOS

Fastest

Low immunity to V_{TH} fluctuation

Replica bias

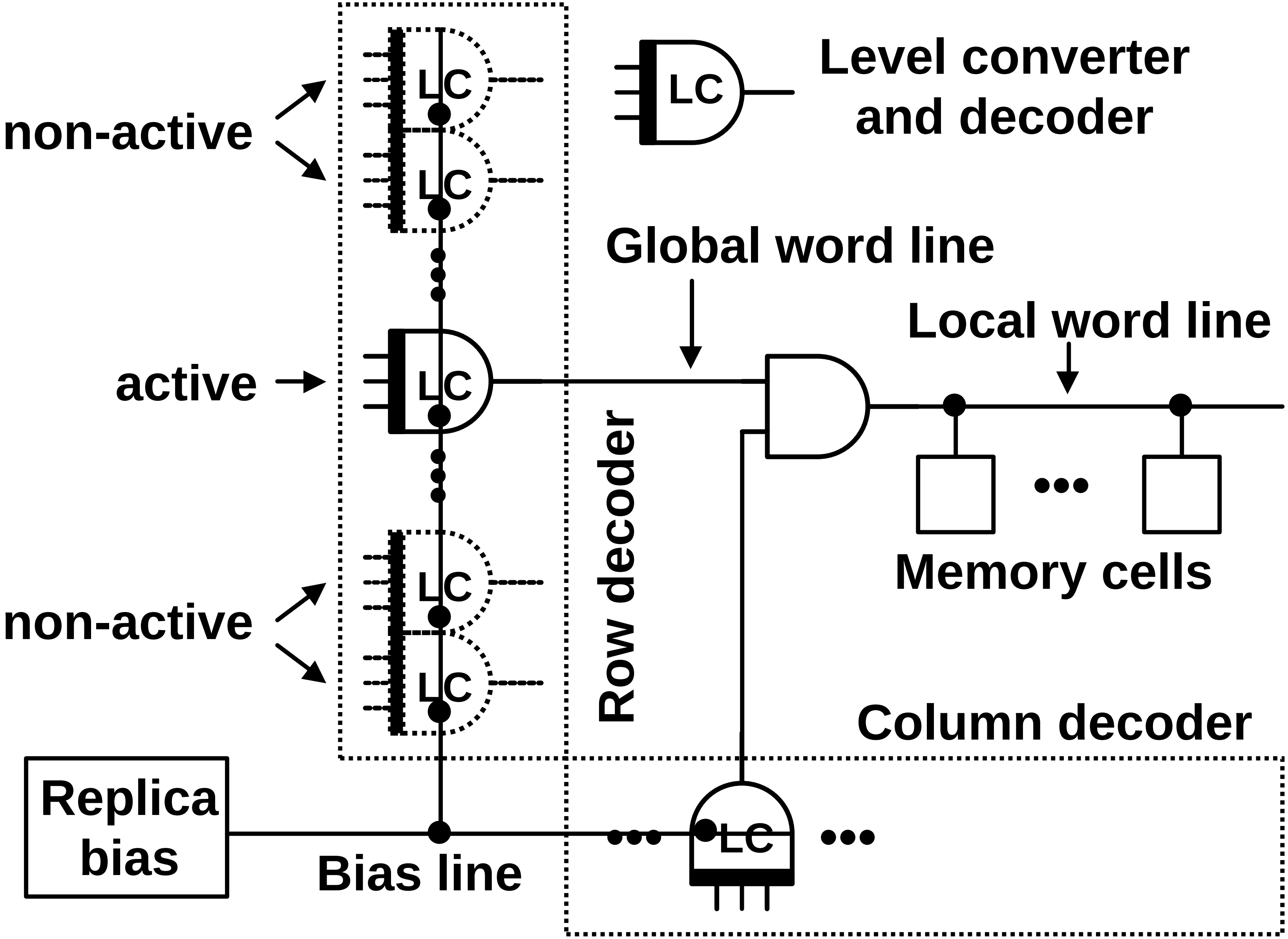
Converter

Replica-biased level converter

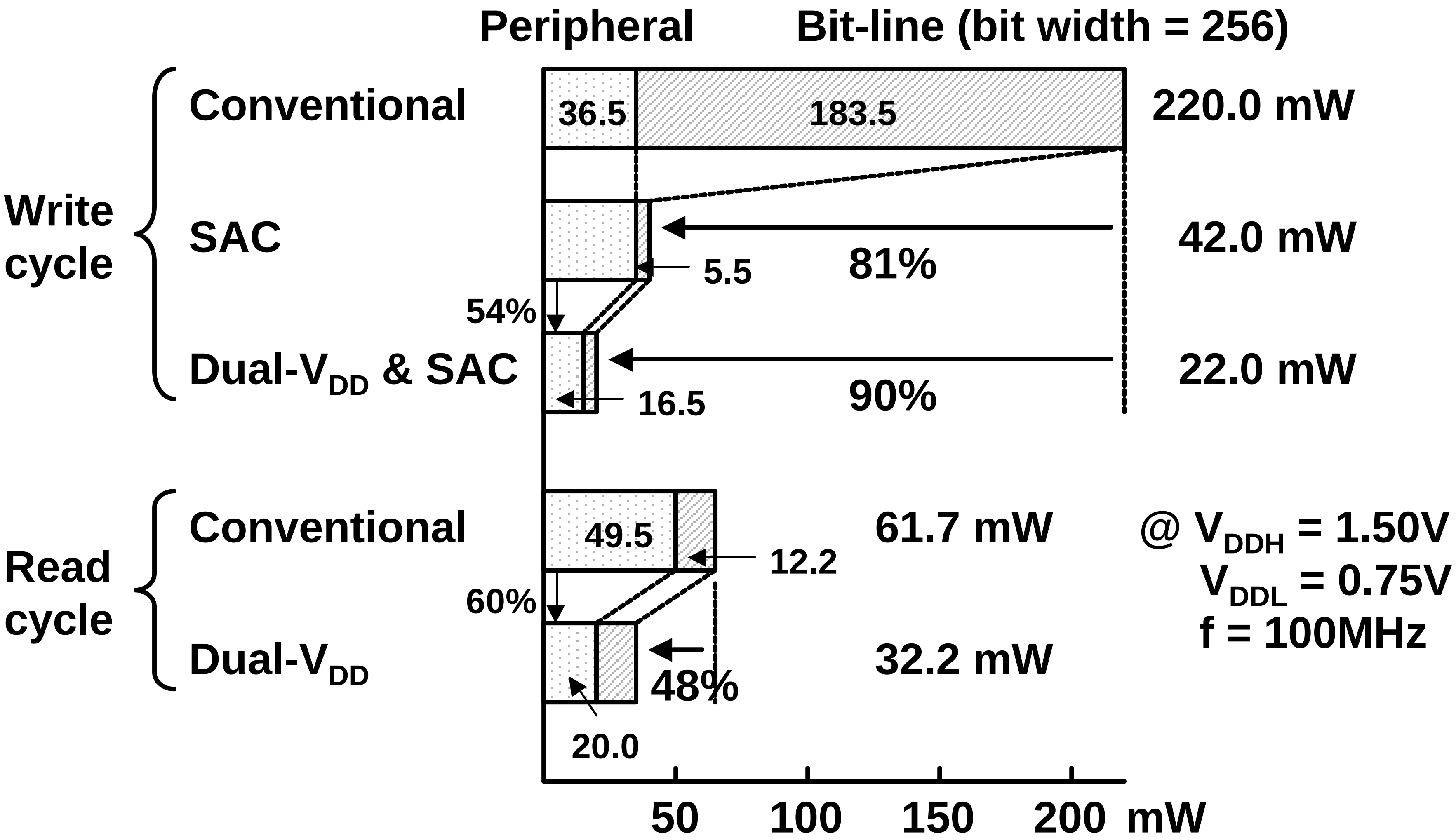
AND gate

High immunity to V_{TH} fluctuation

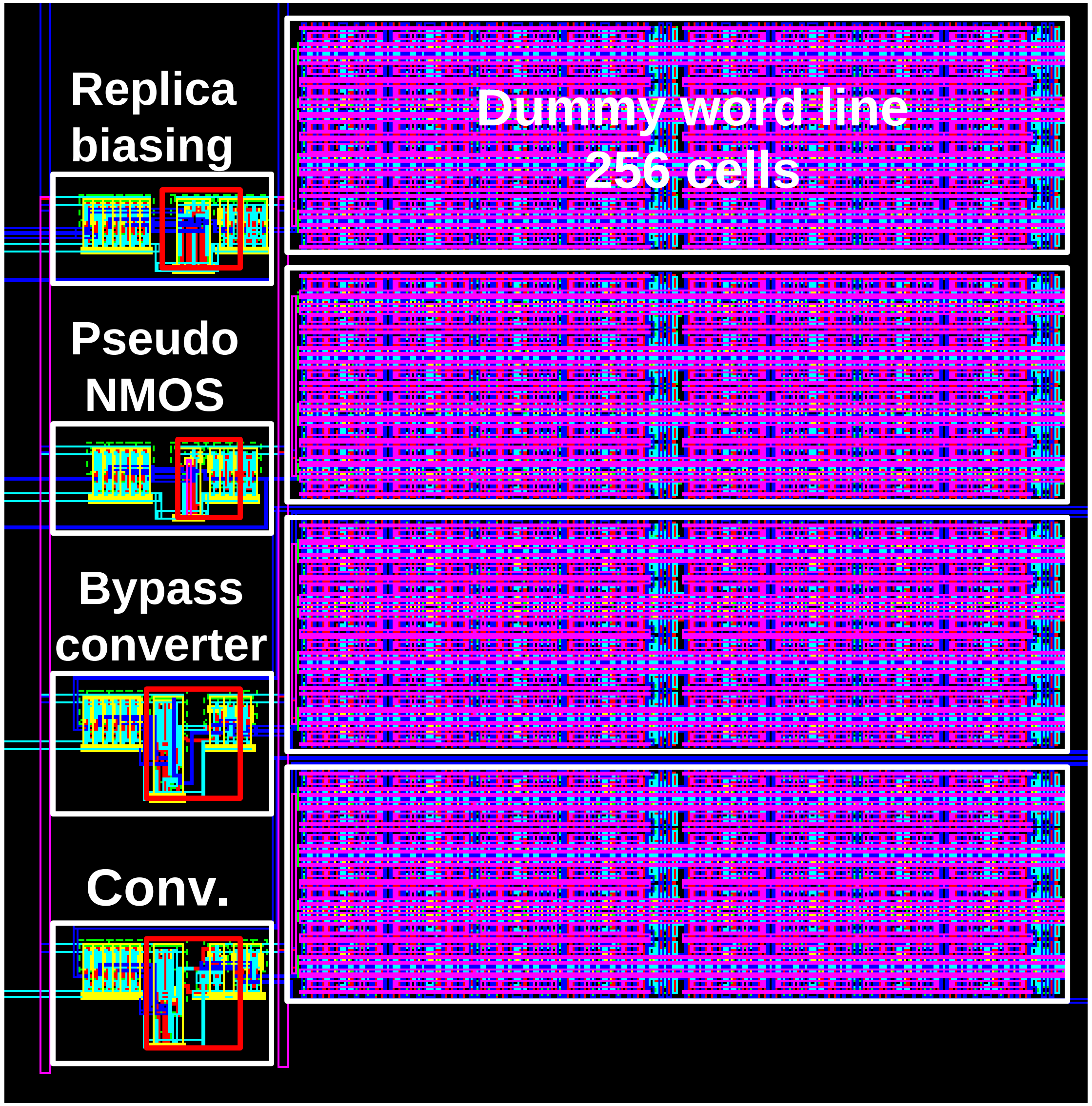
Level converter and decoder



Power consumption of 4Mbit SRAM

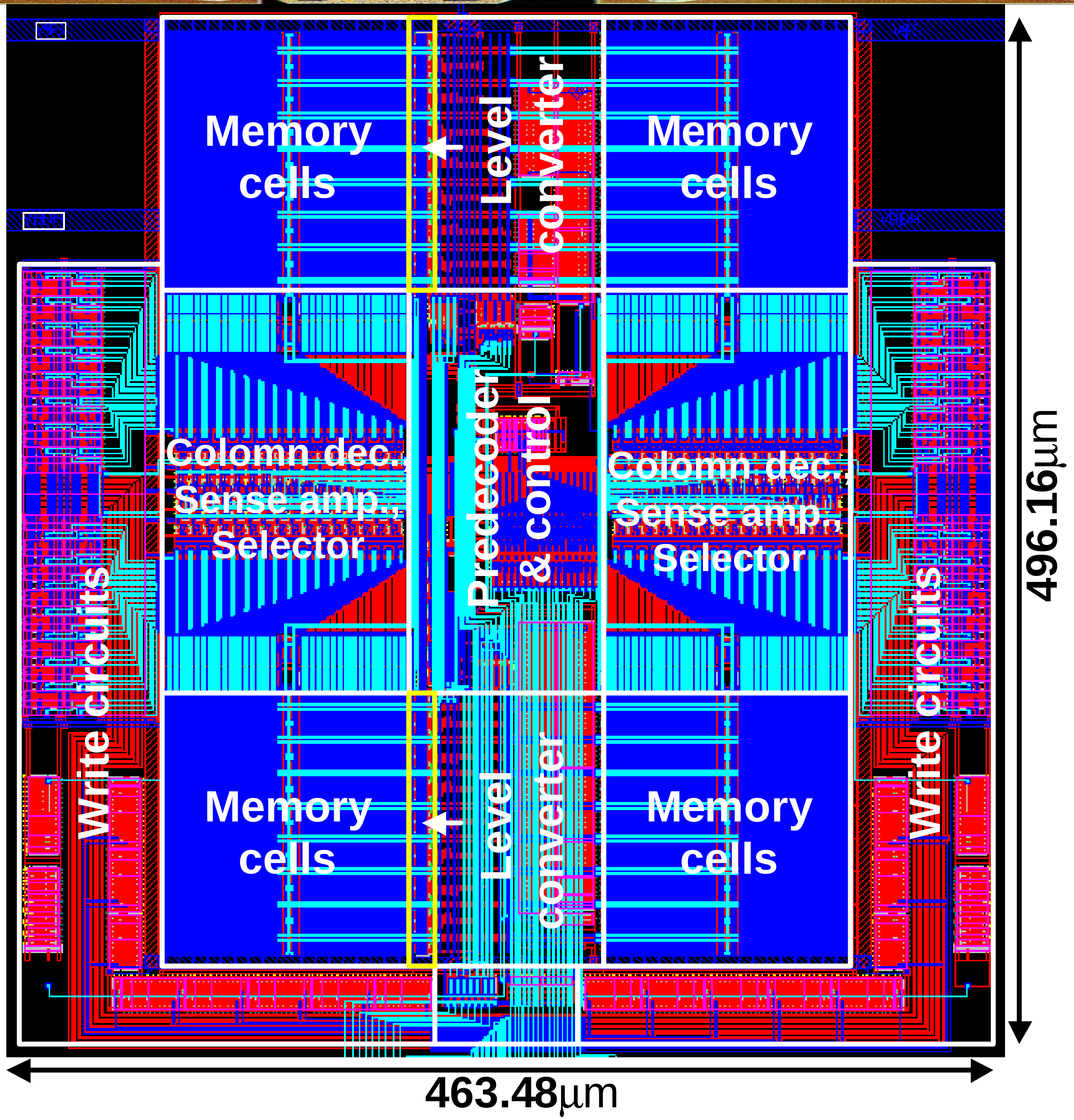


Layout of level converters



Technology:
0.35-μm CMOS
3-metal
(Rohm)

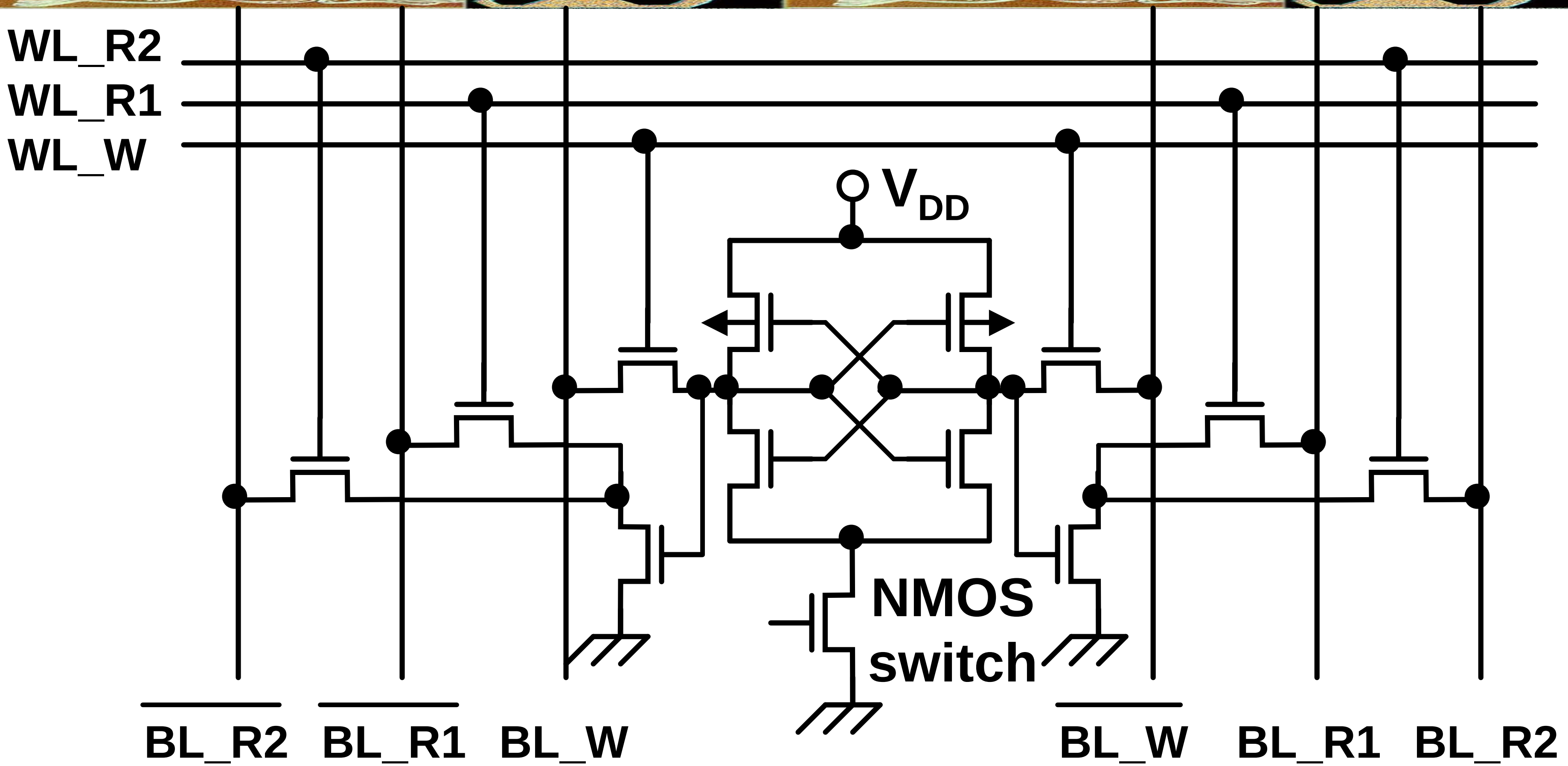
Layout of 2Kbit SRAM with level converter



Technology:
0.25-μm SOI
3-metal
(NEC)

Contents

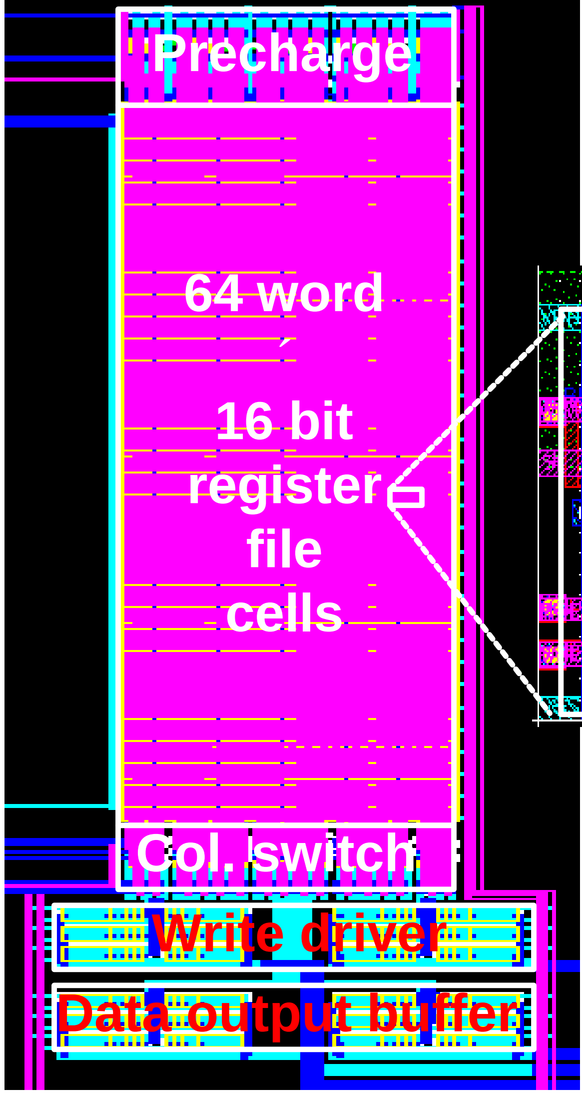
Register file cell with NMOS switch



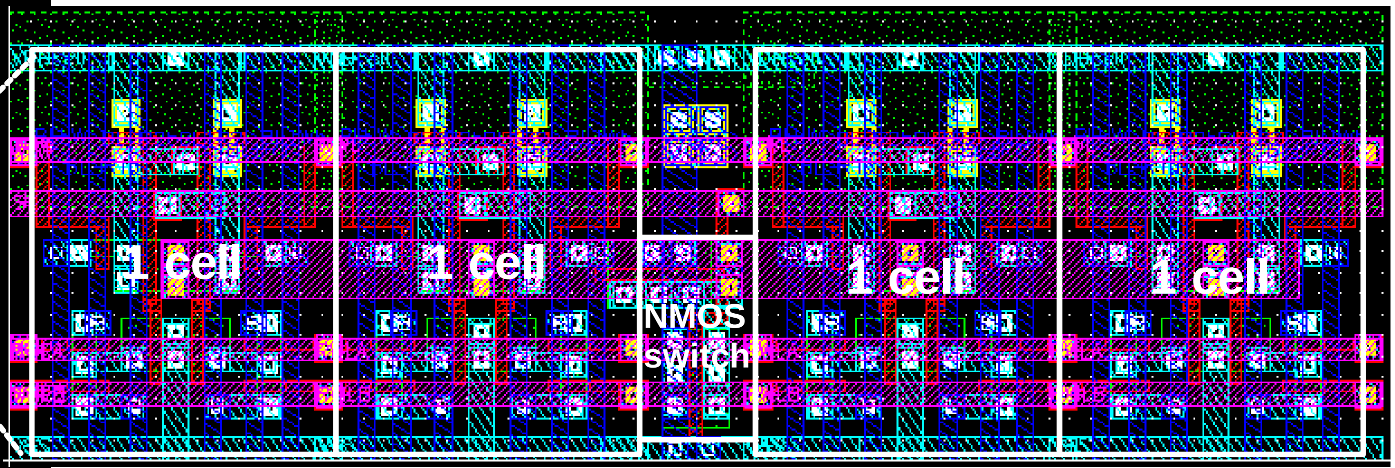
Register file cell with NMOS switch
(one write port and two read ports)

Area overhead is small compared with SRAM

Layout of register file



SAC scheme register file



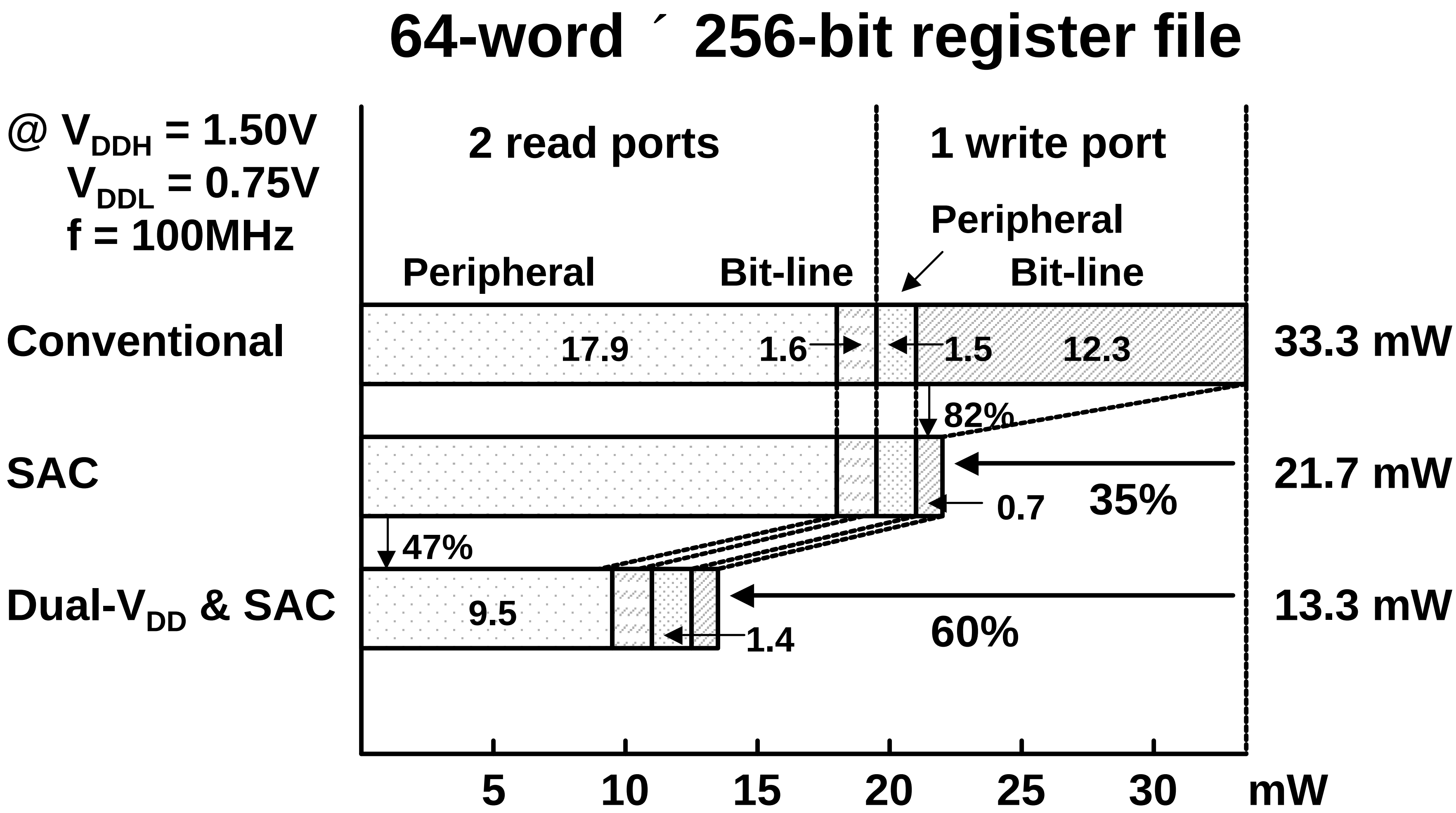
Area overhead 6%-

$$\left(\frac{\text{Area (cell)}}{\text{Area (total)}} = 60\% \right)$$

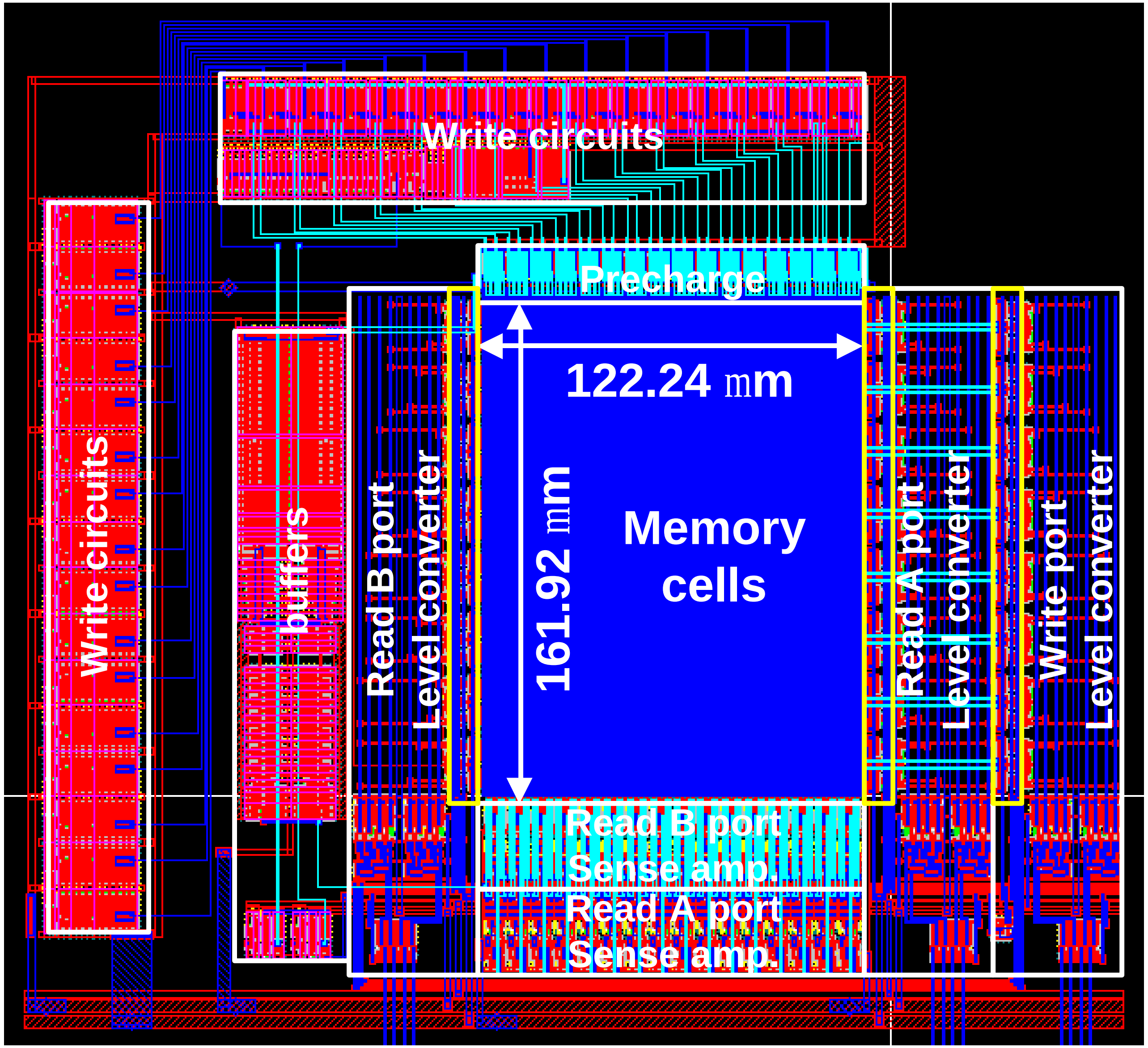
(Area overhead 11%- in SRAM)

Technology:
0.35-μm CMOS 3-metal (Rohm)

Power consumption of register file



Layout of 16-word ´16-bit register file With level converter



Technology:
0.25-mm SOI
3-metal
(NEC)

Summary

Low-power SRAM design

1. Write power saving by SAC scheme
   - ® 81% total write power saving
   - ® 5% delay increase
   - ® 11% area overhead

2. Power saving of peripheral circuits by dual-V_{DD} SRAM architecture
   - ® 54% power saving of peripheral circuits in write cycle
   - ® 90% total write power saving with SAC scheme

3. Application of both schemes to register file
   - ® 60% power saving
   - ® 6% area overhead in SAC scheme