# 低振幅ビット線方式を用いた
# 低消費電力高速SRAM

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# Background

**CMOS power : $P = P_t f_{CLK} C_L V_{DD}^2$ + Leak power**

**Lowering $V_{DD}$ is the best solution to power reduction.**

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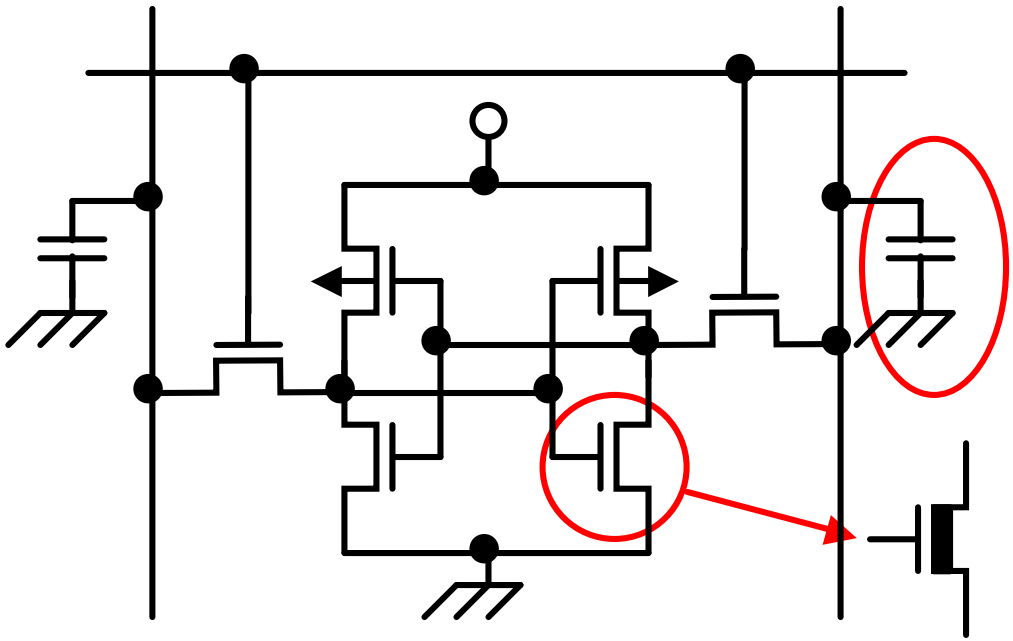
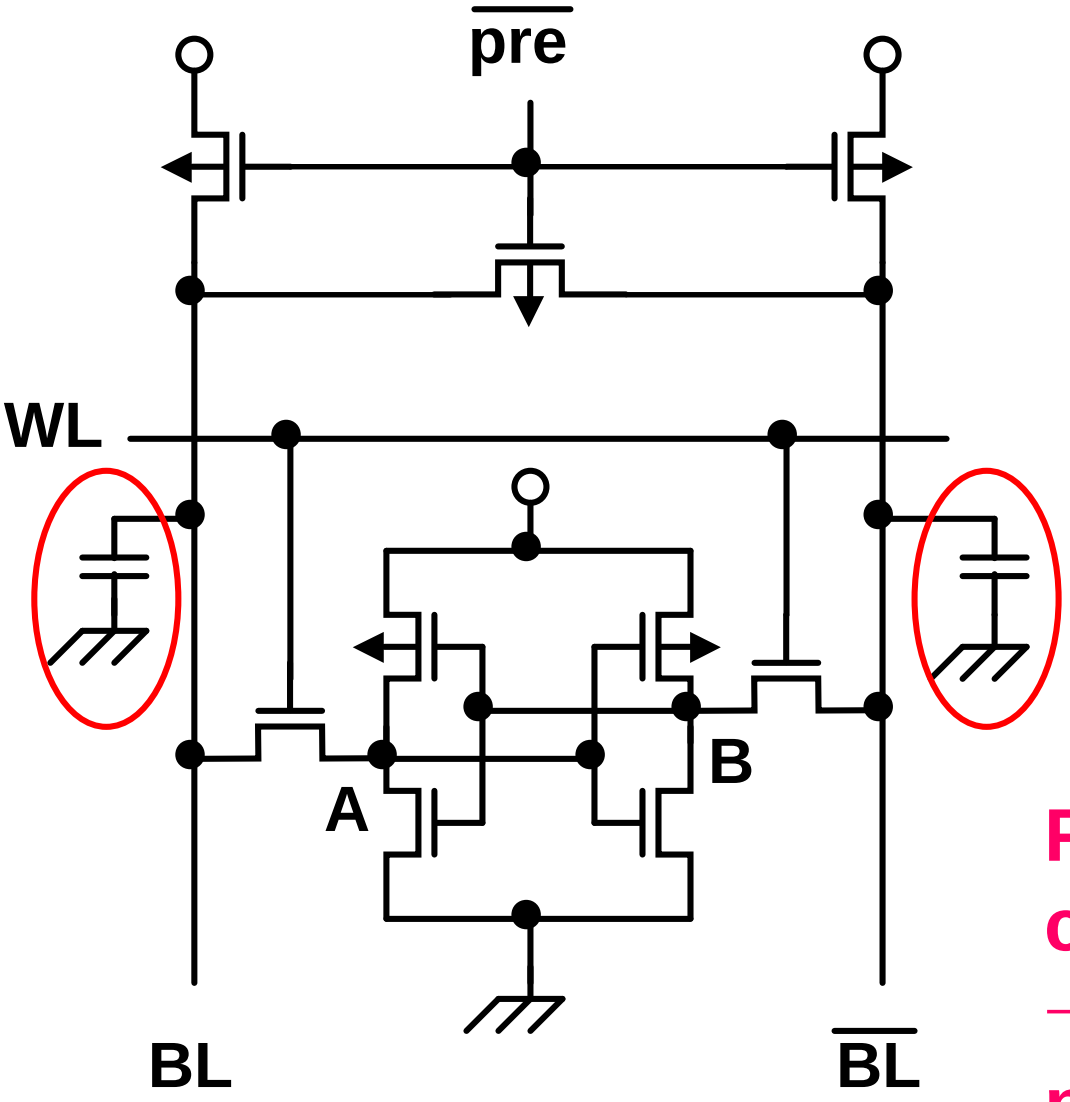
**Lowering $V_{DD}$ of SRAM cell is difficult.**

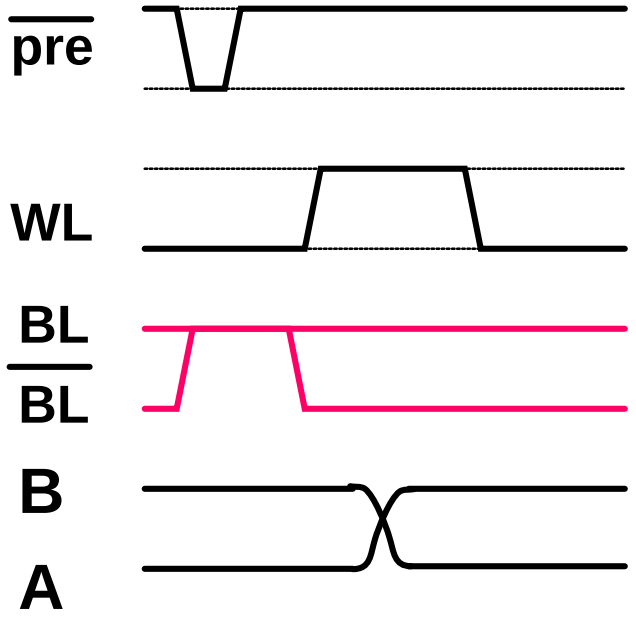


**Large capacitance → Needs strong drivability**

**Low $V_{TH}$ → Leak current**

# Conventional SRAM

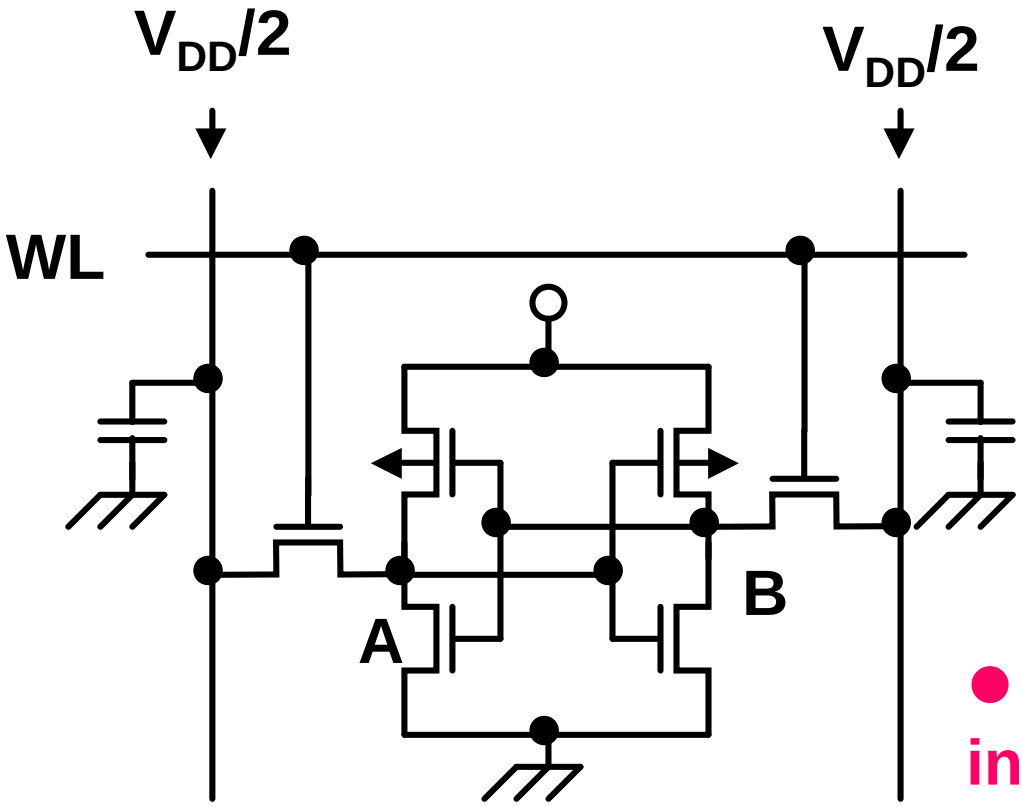


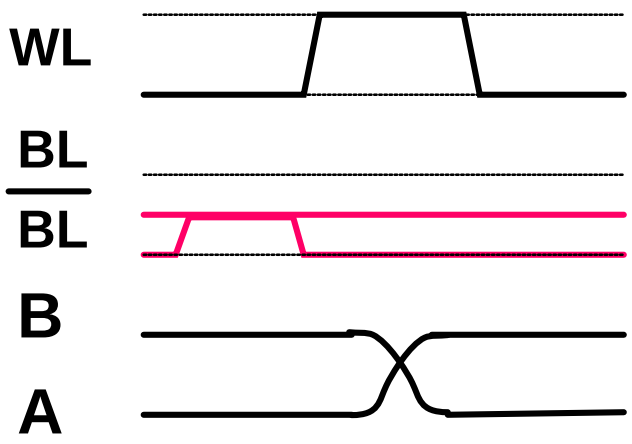




Write-cycle waveform

**Full swing of large capacitance**
**→ Large power at precharge**

# SRAM cell using half-swing bit-lines



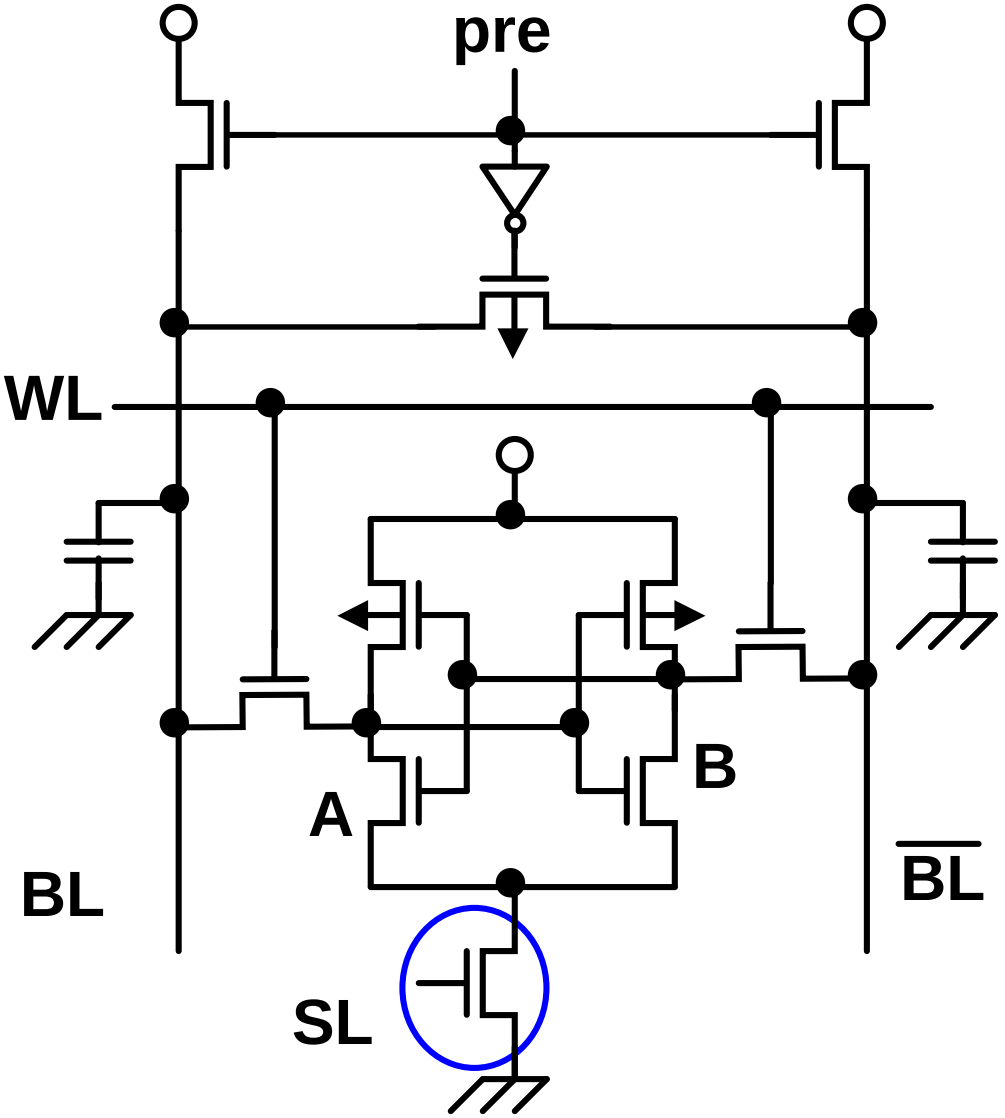



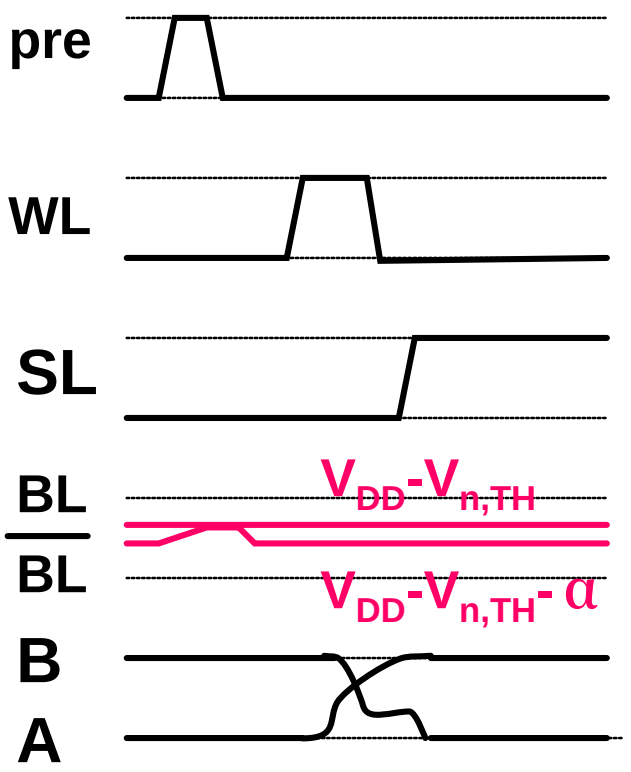

Write-cycle waveform

- Power cannot be saved in write and read cycles.
- Swing level cannot be lowered below $V_{DD}/2$.

(Mark A. Horowitz et al.,
“Low-power SRAM Design Using Half-Swing Pulse-mode Techniques”,
IEEE Journal of SSC, Vol.33, No.11, Nov., 1998)

# SRAM cell using low-swing bit-lines

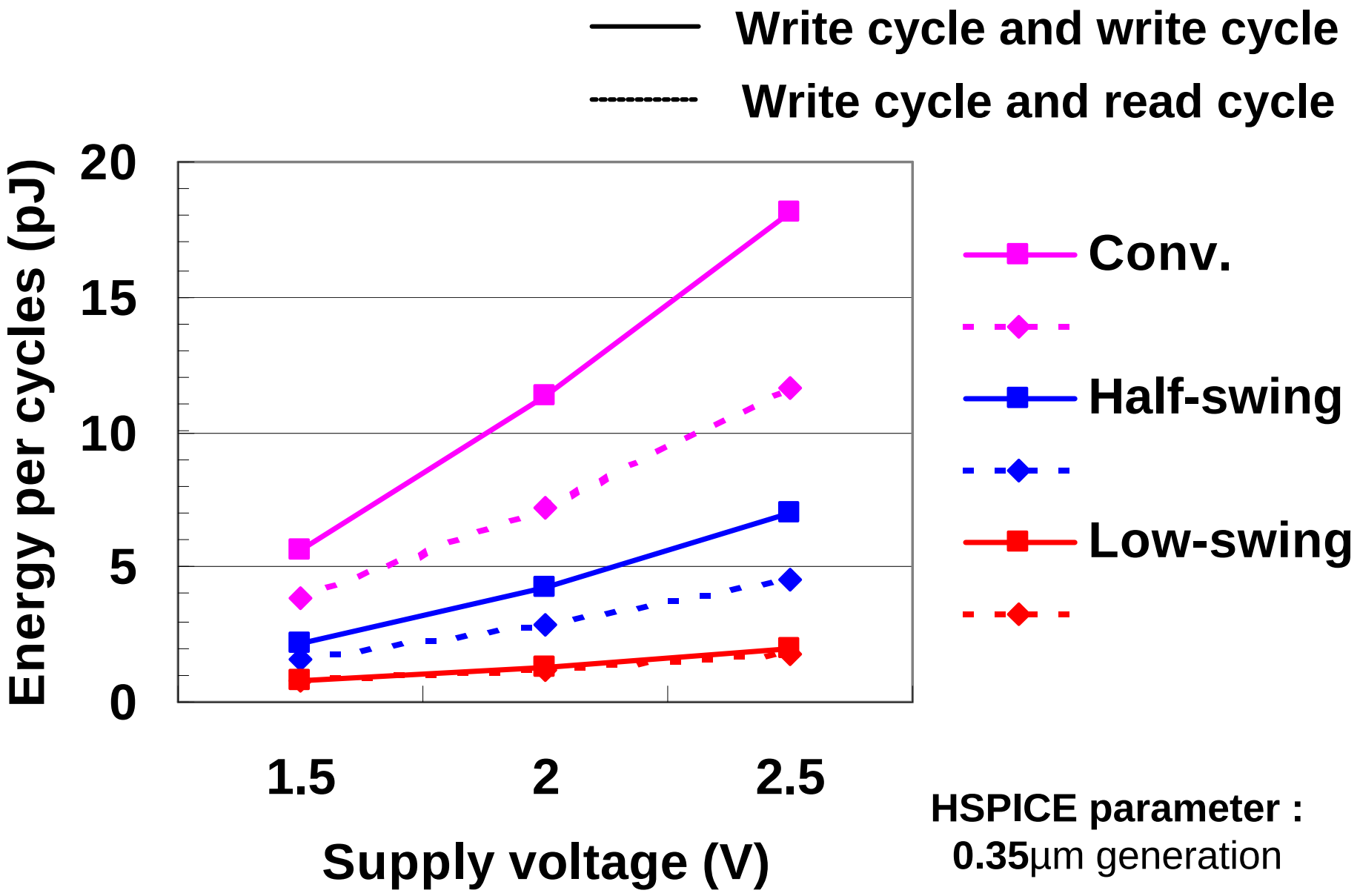



Write-cycle waveform

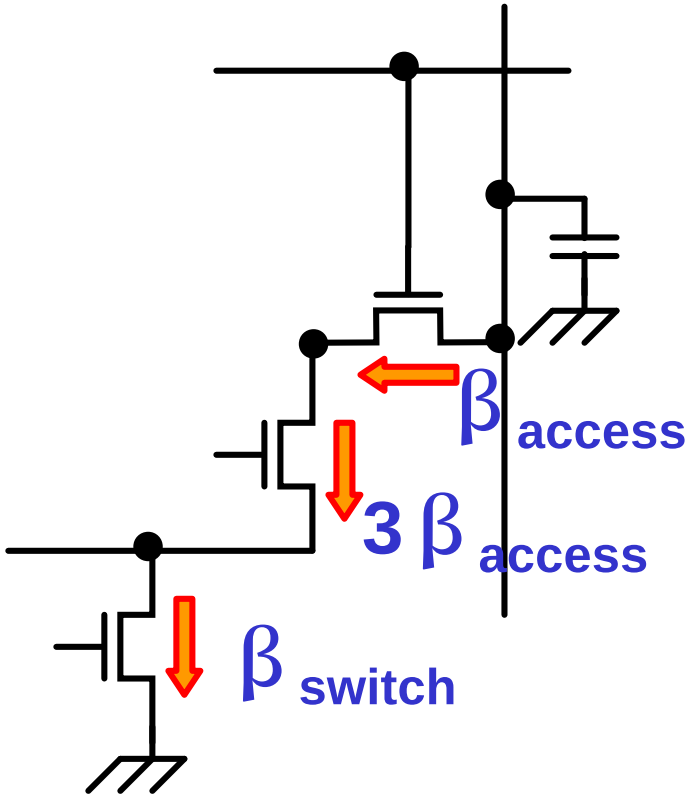
- Power can be saved in write and read cycles.
- Swing level can be lowered below $V_{DD}/2$.

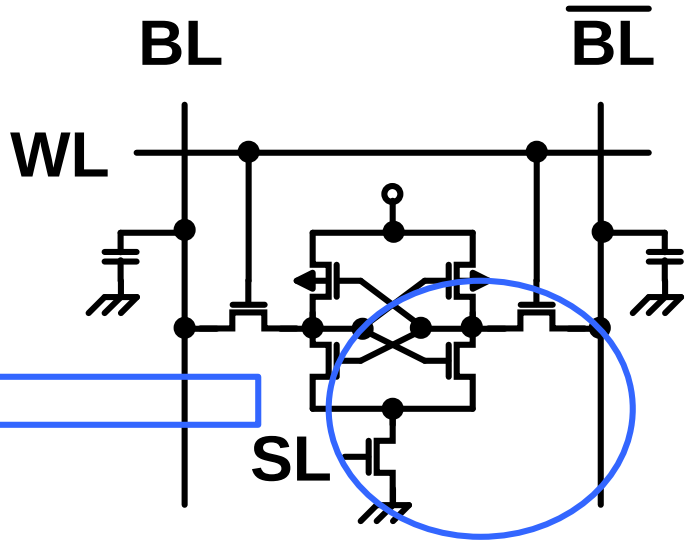
# Simulation result of energy



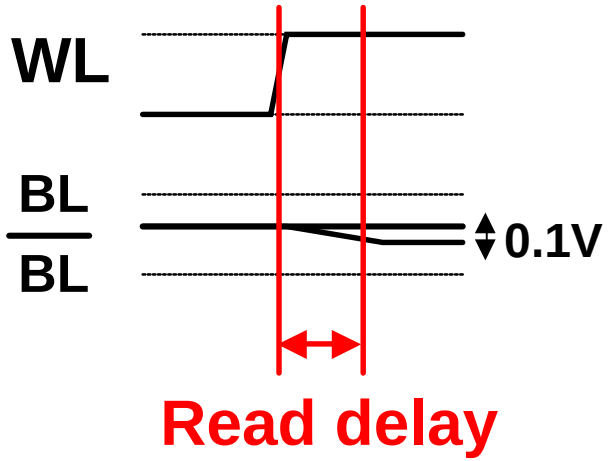

**HSPICE parameter :**
**0.35**μm generation

# Evaluation of read delay

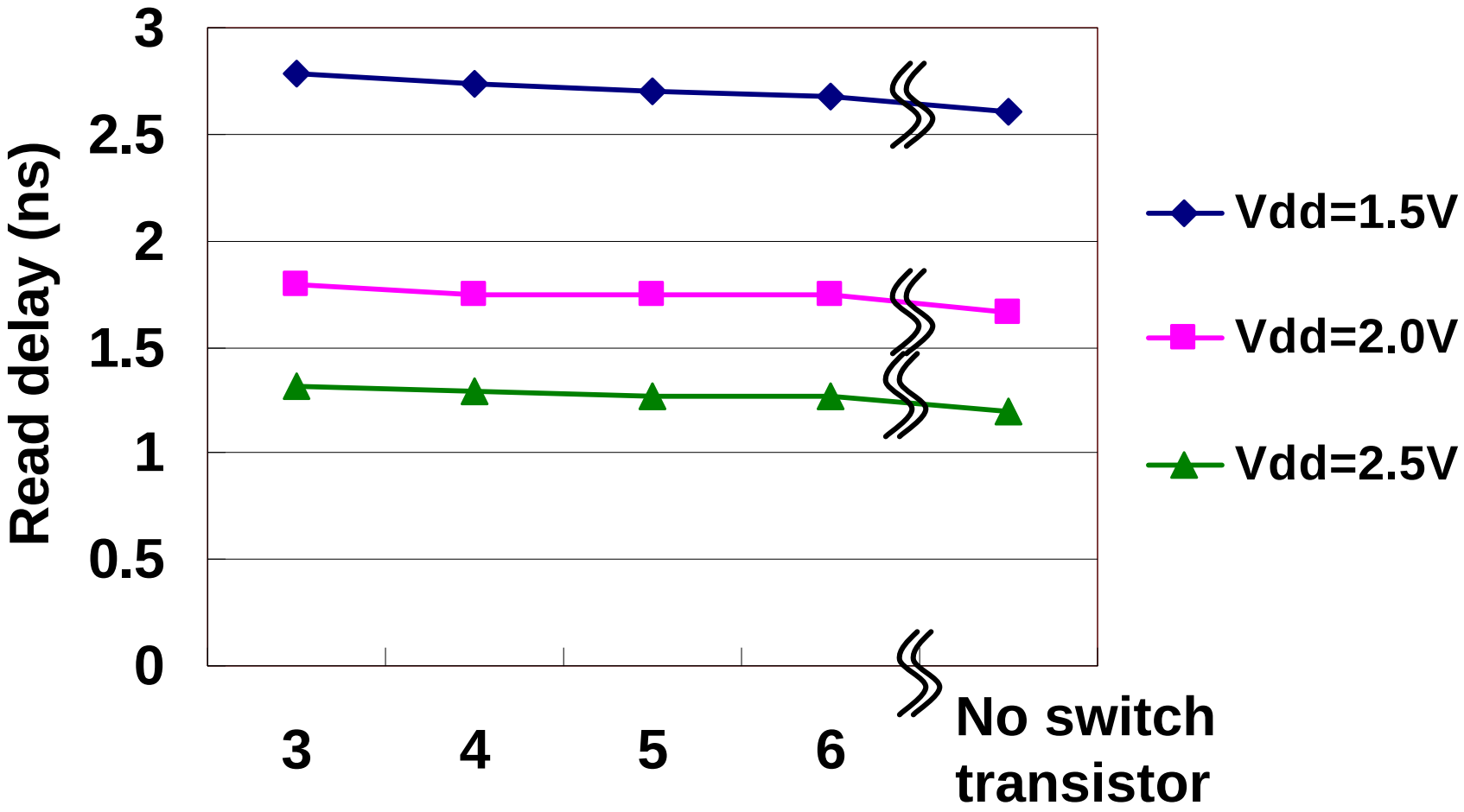



$$\gamma = \frac{\beta_{switch}}{\beta_{access}}$$



# Simulation result of read delay

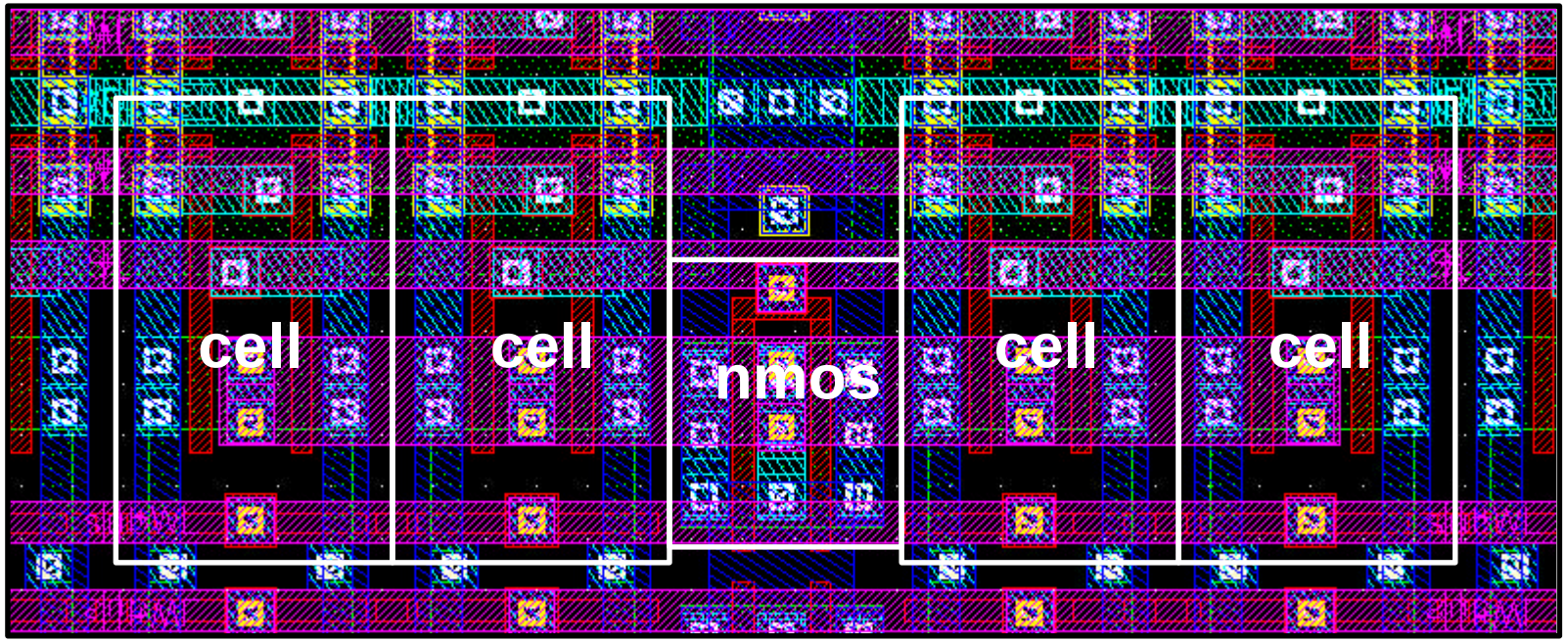



$$\gamma = \beta_{switch} / \beta_{access}$$

**HSPICE parameter :**
**0.35**µm generation

# Layout pattern of SRAM cells

| | |
|---|---|
| Technology | 0.35μm CMOS 3-metal (Rohm) |
| Organization | 256×256 cells |
| Supply voltage | 1.5V～2.5V |
| Core size | 4.0mm² |
| Cell size | 58.5μm² |




**Cell area increases by 17%.**

# Summary

- **SRAM circuits using low-swing bit-lines saves the power by 80% at $V_{DD}$ = 1.5V.**
- **Read delay increases by 7% at $V_{DD}$ = 1.5V.**
- **Cell area increases by 17%.**