高速レベルコンバータ
Bypass Level Converter (BLC)

第62回応用物理学会学術講演会

東京大学生産技術研究所
服部 貞昭　神田 浩一　桜井貴康

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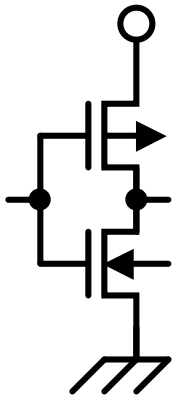
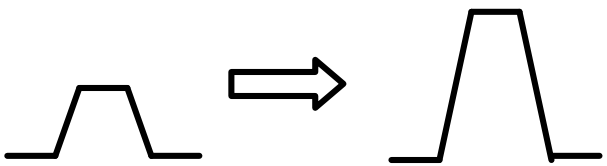
Background



CMOS active power : $P = P_t f_{CLK} C_L V_{DD}^2$

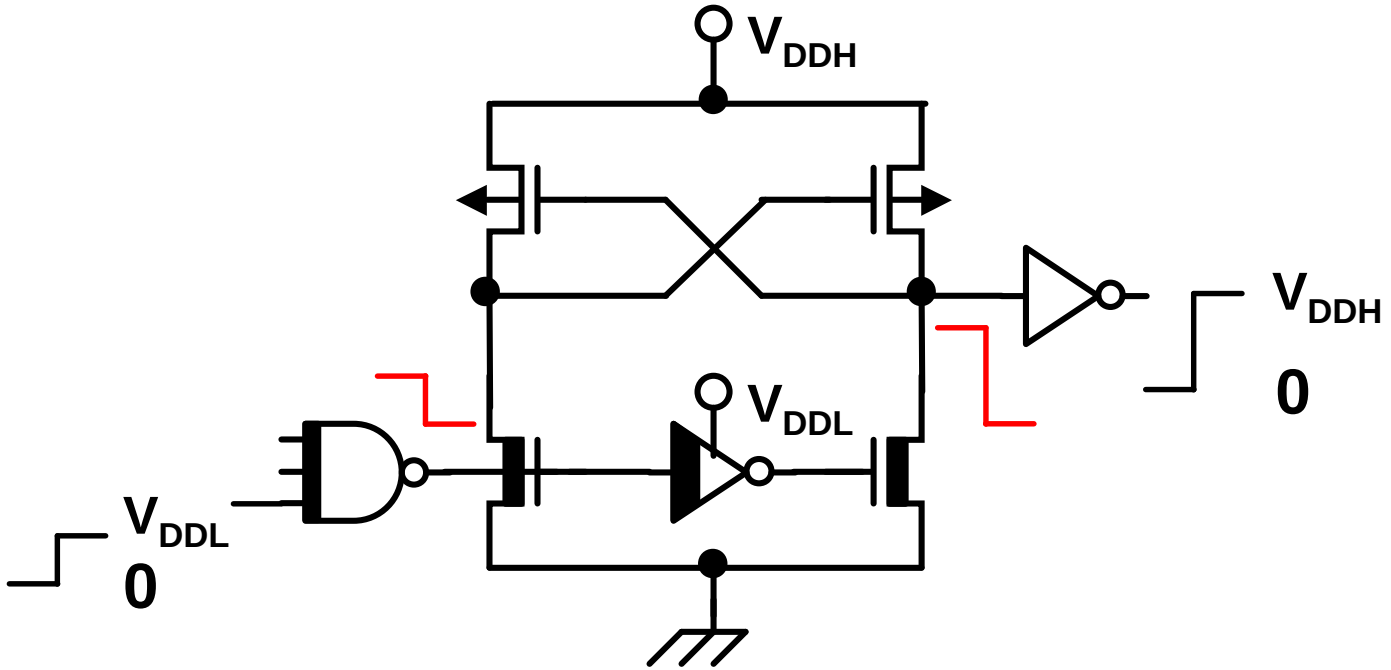
Lowering V_{DD} is the best solution to power reduction.

High voltage is also required for memory and Input/Output.



High speed level converter for low voltage operation is required.

Conventional level converter



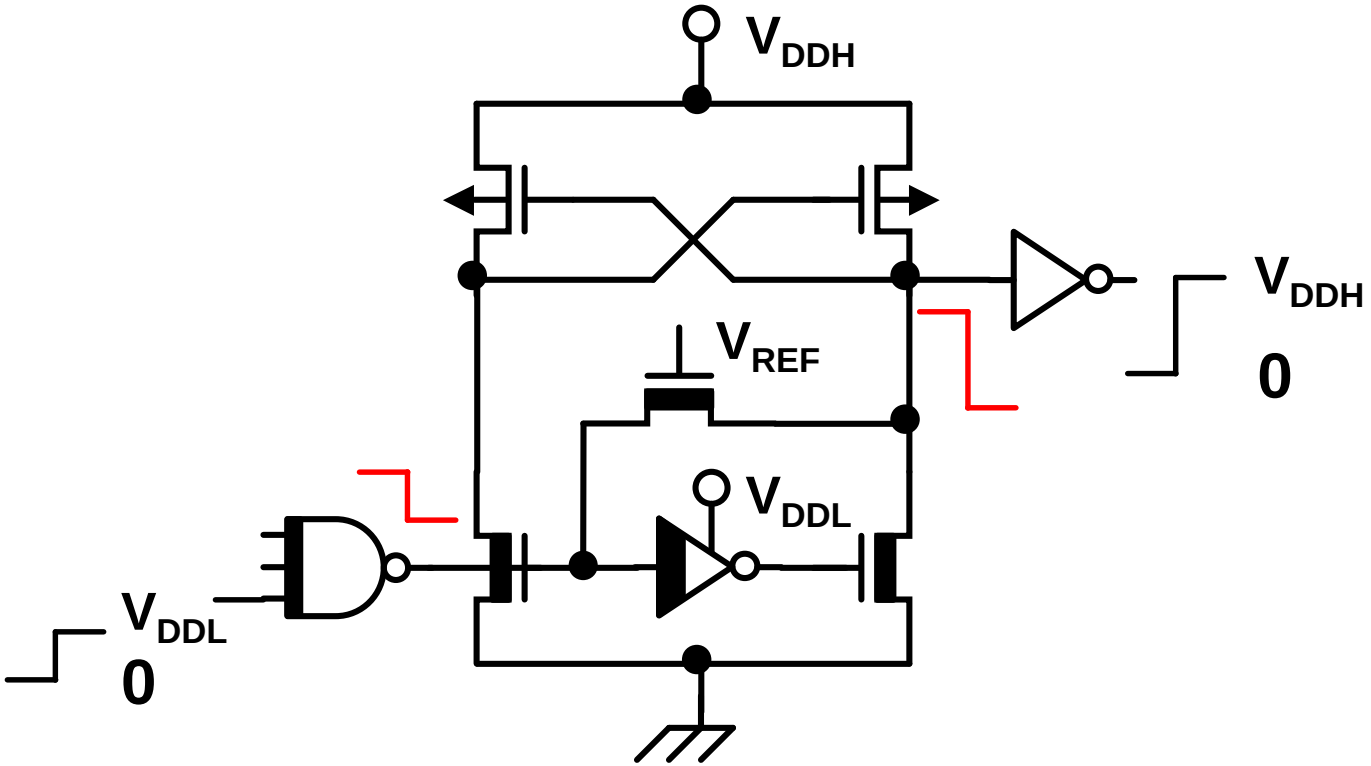
High-V_{TH} MOS : $V_{TH, HIGH}$

Low-V_{TH} MOS : $V_{TH, LOW}$

V_{DDH} : High V_{DD}

V_{DDL} : Low V_{DD}

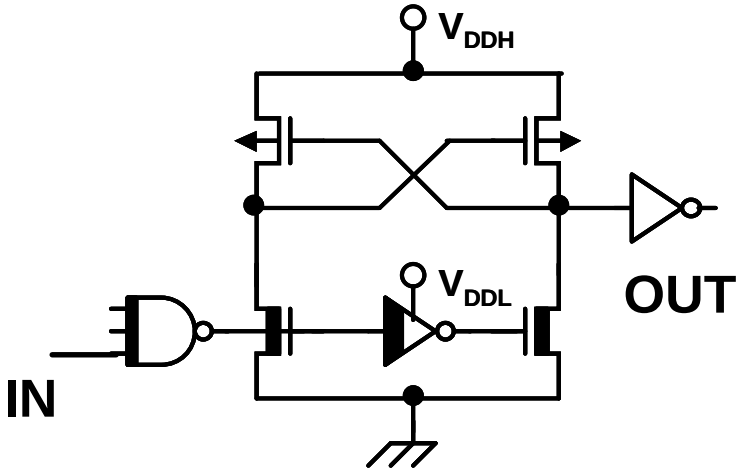
Proposed level converter



V_{REF} : Reference voltage

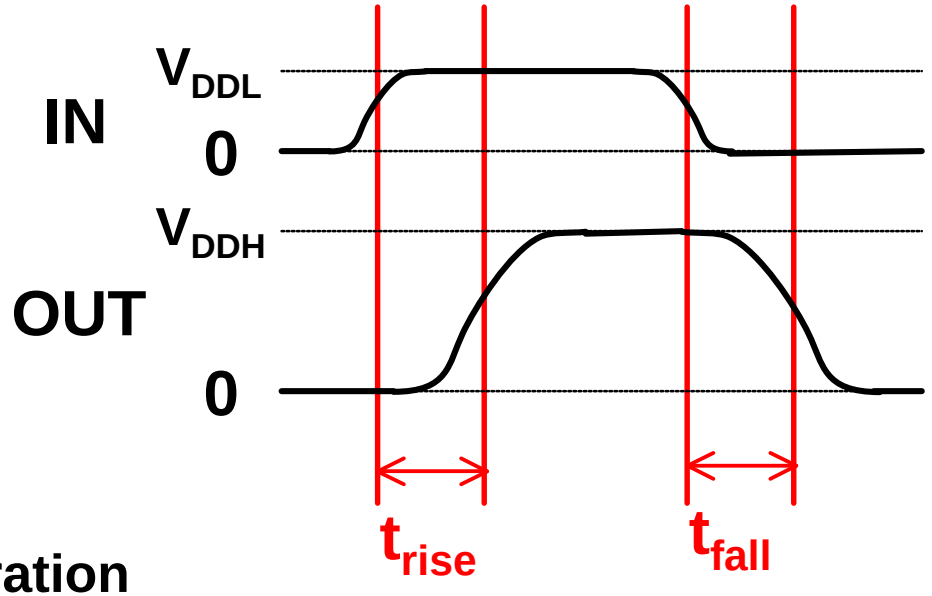
$= V_{DDL} + V_{TH,\,LOW} - 0.1V$

Simulation method



V_{DDH} = 1.0V, 1.5V, 2.0V
V_{DDL} = 0.5

$V_{TH, HIGH}$ = 0.39V
$V_{TH, LOW}$ = 0.09V ~ 0.39V

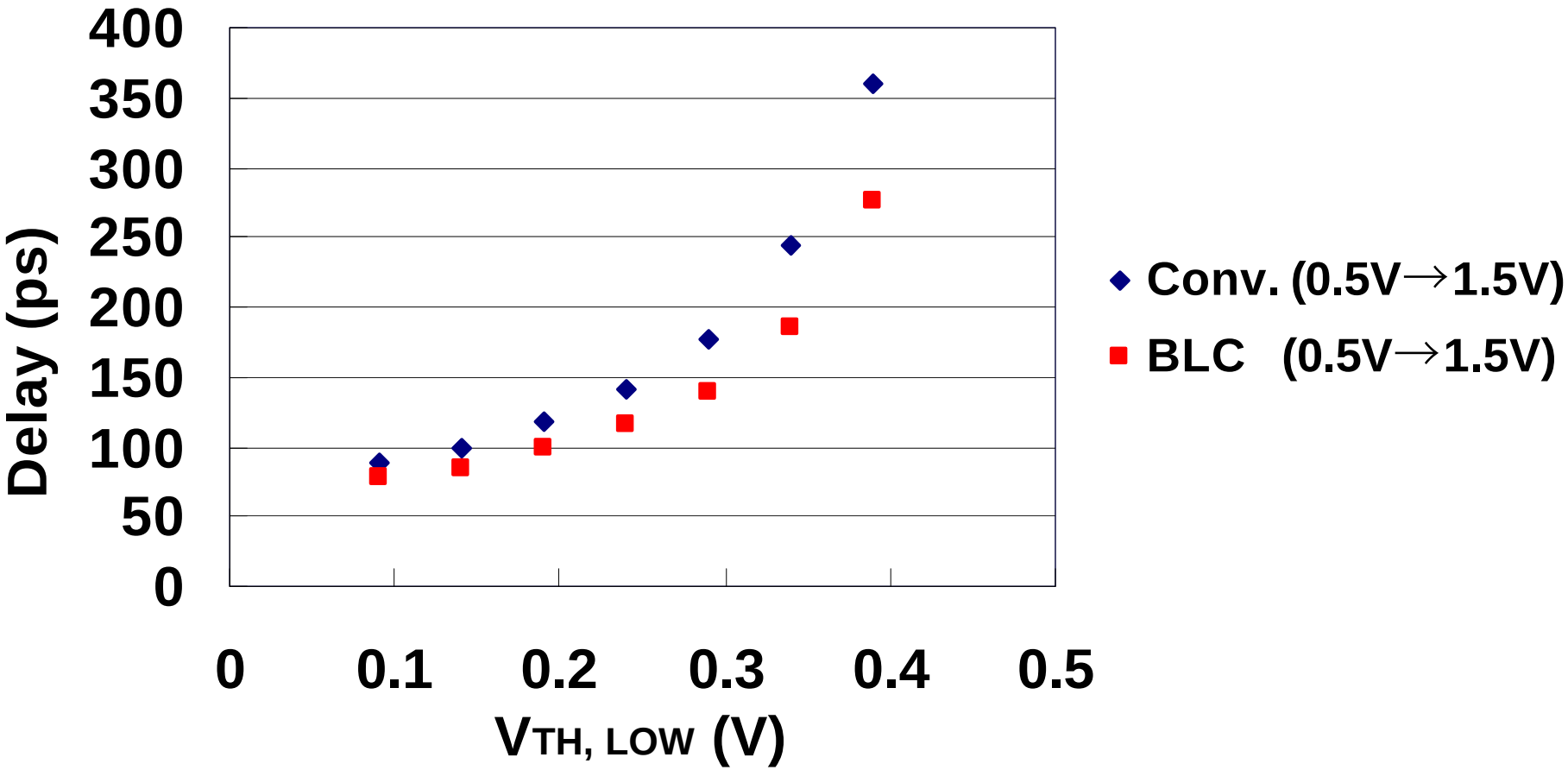


Widths of all the transistors are optimized so that $t_{rise} = t_{fall} = min$.

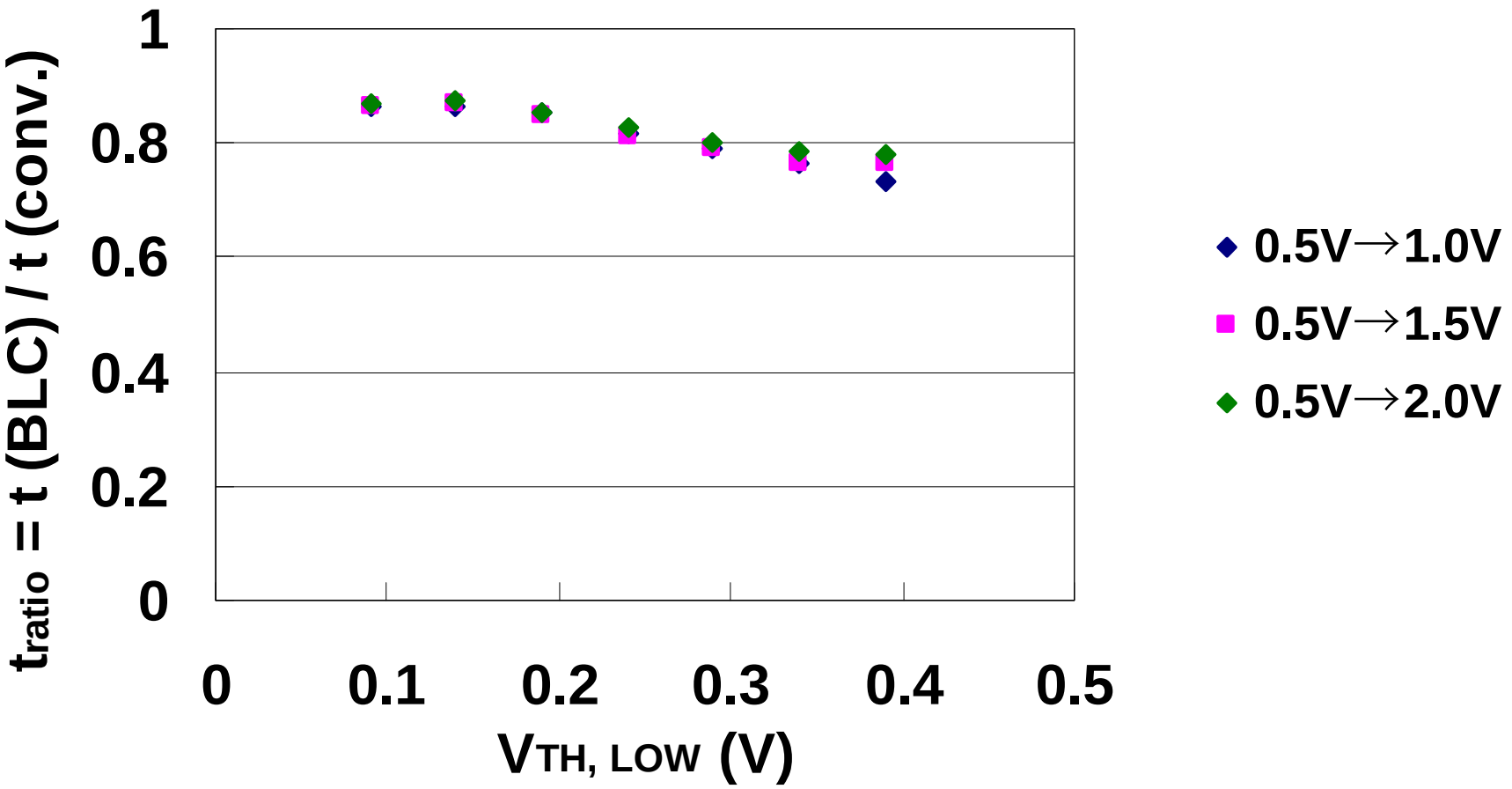
HSPICE parameter : 0.13μm generation

稲垣賢一・神田浩一・桜井貴康, "ITRSロードマップ準拠標準SPICEモデルの構築," 2000年電子情報通信学会ソサイエティ大会, A-3-7, 2000年10月

Simulation result of delay

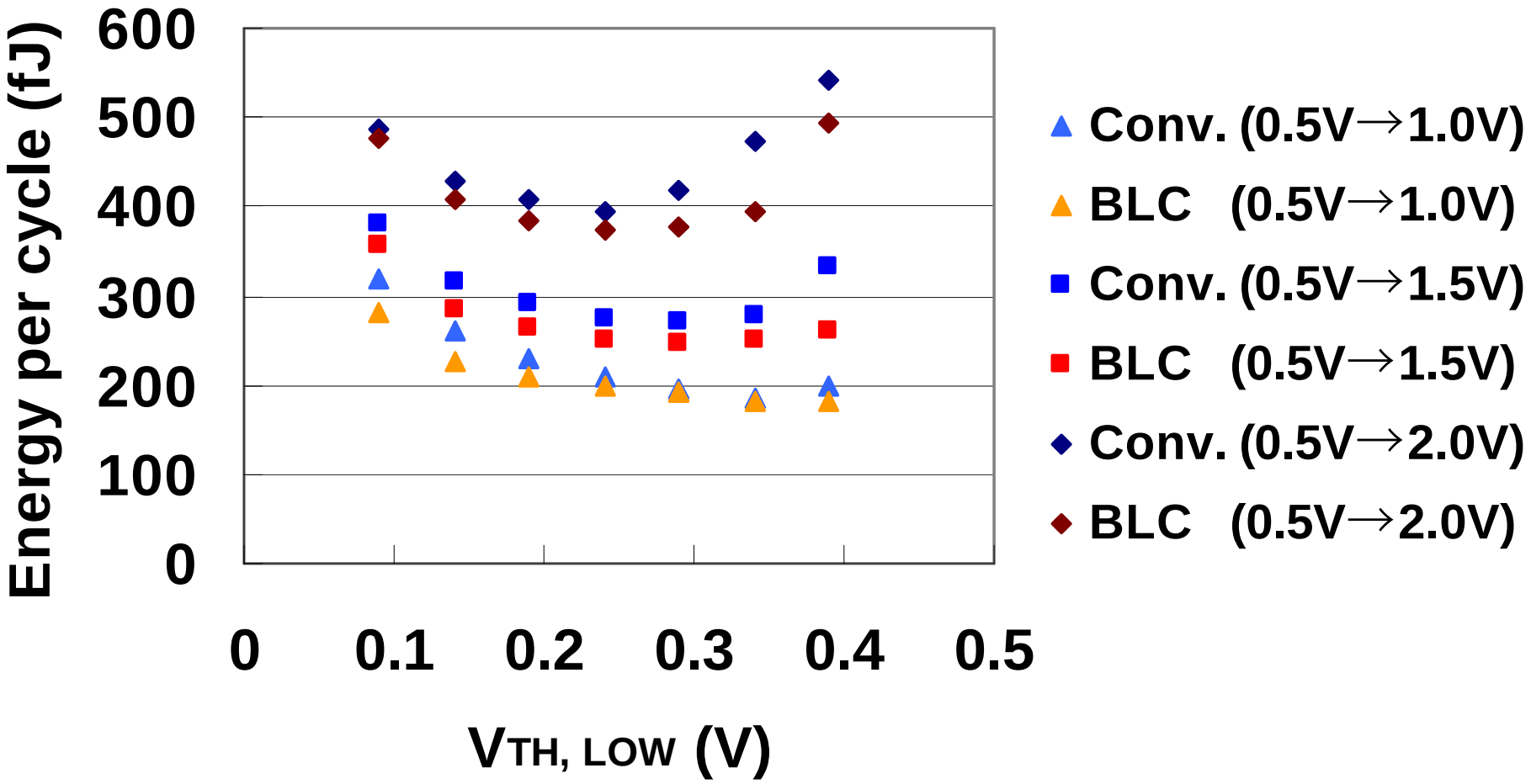


Simulation result of delay



$$t_{ratio} = \frac{t_{rise},\ t_{fall} \text{ of proposed converter}}{t_{rise},\ t_{fall} \text{ of bypass level converter}}$$

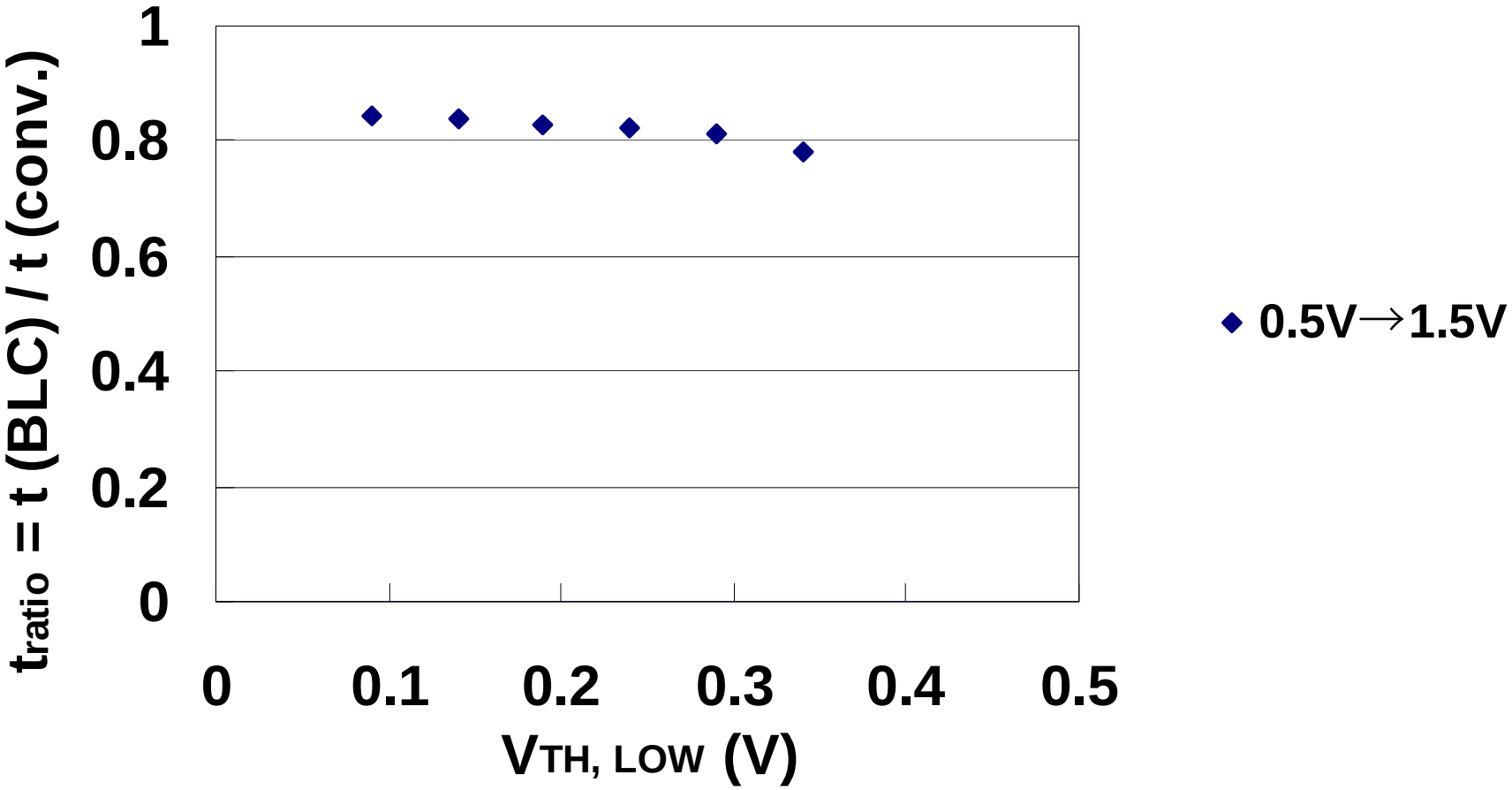
Simulation result of power



Summary

- **Proposed bypass level converter (BLC) reduces the delay by 15% when $V_{TH,\ low}$ = 0.19V.**
- **BLC reduces the power by 10% when $V_{TH,\ low}$ = 0.19V.**

Simulation result of delay



HSPICE parameter : 0.07μm generation